

# Nanotech

Conference & Expo 2009



## Workshop on Compact Modeling

*Chair: Xing Zhou*



# Workshop on Compact Modeling

## Tuesday May 5

- 8:30 WCM Keynote – What is a Transistor?
- 9:10 Interface Traps in Surface-Potential-Based MOSFET Models
- 9:30 Analytic MOSFET Surface Potential Model with Inclusion of Poly-Gate Accumulation, Depletion, and Inversion Effects
- 10:30 HiSIM-SOI: SOI-MOSFET Model for Circuit Simulation Valid also for Device Optimization
- 10:50 Embedded non-volatile memory study with surface potential based model
- 11:10 Dynamic Charge Sharing modeling for surface potential based models
- 11:30 Effective Width Modeling for Body-Contacted Devices in Silicon-On-Insulator Technology
- 1:30 Charge-based compact modeling techniques for nanoscale Multi-Gate MOSFETs
- 1:50 Design study of CNT transistors layouts for high frequency analog circuits
- 2:10 Analytical Modelling of Ballistic and Quasi-Ballistic Nanowires: Validation and Application to CMOS Architecture
- 3:30 Compact Quantum Modeling Framework for Nanoscale Double-Gate MOSFET
- 3:50 Compact Model HiSIM-DG both for Symmetrical and Asymmetrical DG-MOSFET Structures
- 4:10 A Unified Compact model for FinFET and Silicon Nanowire MOSFETs
- 4:30 Computation Efficient yet Accurate Surface Potential Based Analytic Model for Symmetric DG MOSFETs to Predict Current-Voltage Characteristics
- 4:50 Compact Modeling of Dynamic Threshold Voltage of FinFET High K Gate Stack and Application in Circuit Simulation

# Workshop on Compact Modeling

## Wednesday May 6

- 8:30 High-Voltage MOSFET Model Valid for Device Optimization
- 8:50 Compare and Contrast HiSIM-LDMOS and BSIM based compact model of High Voltage MOSFETs for Analog Applications
- 9:10 A Scalable POWER MOSFET Model with an Integrated Body-Diode Including Reverse Recovery
- 9:30 A PSpice Compact Model for Organic Field-Effect Transistors
- 10:30 Compact Model Application to Statistical/Probabilistic Technology Variations
- 10:50 Elements of Statistical SPICE Models
- 11:10 PSP Model Equations Extension for Statistical Estimation of Leakage Current in Nanometer CMOS Technologies Considering Process Variations
- 1:30 RF Modeling of 45nm Low-Power CMOS Technology
- 1:50 Compact Model of Low – Frequency Noise in Nanoscale Metal-Oxide-Semiconductor Field Effect Transistors
- 2:10 1/f Noise Modeling at Low Temperature with the EKV3 Compact Model
- 2:30 1/f Noise Model for Double-Gate FinFET Biased in Weak Inversion
- 2:50 A Simple, Accurate Capacitance-Voltage Model of Undoped Silicon Nanowire MOSFETs
- 3:50 SPICE BSIM3 Model Parameters Extraction and Optimization for Low Temperature Application
- 4:10 An SOA Aware MOSFET Model for Highly Integrated, Analog Mixed-Signal Design Environments
- 4:30 Automatically Generated and Experimentally Validated System-Level Model of a Microelectromechanical RF Switch

# WCM: Bulk MOS models

Tue, 8:30am. Session chair: Xing Zhou

- **WCM Keynote: What Is a Transistor?**

Chih-Tang Sah, B. Jie, *University of Florida, US*

- **Interface Traps in Surface-Potential-Based MOSFET Models**

Z. Chen, X. Zhou, G.H. See, Z. Zhu, G. Zhu, *Nanyang Technological University, SG*

- **Analytic MOSFET Surface Potential Model with Inclusion of Poly-Gate Accumulation, Depletion, and Inversion Effects**

Y. Song, J. He, L.N. Zhang, J. Zhang, *Peking University, CN*

# WCM: Bulk/SOI models

Tue, 10:30am. Session chair: Xing Zhou

- **HiSIM-SOI: SOI-MOSFET Model for Circuit Simulation Valid also for Device Optimization**

N. Sadachika, S. Kusu, K. Ishimura, T. Murakami, T. Kajiwara, T. Hayashi, Y. Nishikawa, T. Yoshida, M. Miura-Mattausch, *Hiroshima University, JP*

- **Embedded non-volatile memory study with surface potential based model**

D. Garetto, A. Zaka, V. Quenette, D. Rideau, E. Dornel, W.F. Clark, M. Minondo, C. Tavernier, Q. Rafhay, R. Clerc, A. Schmid, Y. Leblebici, H. Jaouen, *STMicroelectronics, FR*

- **Dynamic Charge Sharing modeling for surface potential based models**

V. Quenette, D. Rideau, R. Clerc, C. Tavernier, H. Jaouen, *STMicroelectronics, FR*

- **Effective Width Modeling for Body-Contacted Devices in Silicon-On-Insulator Technology**

S. Khandelwal, E. Tamilmani, K. Shanbhag, J. Watts, *IBM SRDC Bangalore, IN*

## **WCM: Multi-gate/nanowire/nanotube models**

Tue, 1:30pm. Session chair: Bin Jie

- **Charge-based compact modeling techniques for nanoscale Multi-Gate MOSFETs**  
B. Iñiguez, F. Lime, A. Lázaro, O. Moldovan, B. Nae,  
*Universitat Rovira i Virgili, ES*
- **Design study of CNT transistors layouts for high frequency analog circuits**  
M. Claus, M. Schröter, *Technische Universität Dresden, DE*
- **Analytical Modelling of Ballistic and Quasi-Ballistic Nanowires: Validation and Application to CMOS Architecture**  
S. Martinie, D. Munteanu, G. Le Carval, M.-A. Jaud, J.L. Autran, *CEA, LETI, Minatec, FR*

# WCM: Double-gate models

Tue, 3:30pm. Session chair: François Lime

- **Compact Quantum Modeling Framework for Nanoscale Double-Gate MOSFET**  
*U. Monga, T.A. Fjeldly, Norwegian University of Science and Technology, NO*
- **Compact Model HiSIM-DG both for Symmetrical and Asymmetrical DG-MOSFET Structures**  
*K. Ishimura, N. Sadachika, S. Kusu, M. Miura-Mattausch, Hiroshima University, JP*
- **A Unified Compact model for FinFET and Silicon Nanowire MOSFETs**  
*G.J. Zhu, X. Zhou, G.H. See, S.H. Lin, C.Q. Wei, J.B. Zhang, Nanyang Technological University, SG*
- **Computation Efficient yet Accurate Surface Potential Based Analytic Model for Symmetric DG MOSFETs to Predict Current-Voltage Characteristics**  
*Y. Song, L.N. Zhang, J. Zhang, H. Zhuang, Y.C. Che, J. He, M. Chan, Peking University, CN*
- **Compact Modeling of Dynamic Threshold Voltage of FinFET High K Gate Stack and Application in Circuit Simulation**  
*F. He, C. Ma, B. Li, L. Zhang, X. Zhang, X. Lin, SZPKU, CN*

# WCM: HV/LDMOS/OFET models

Wed, 8:30am. Session chair: Xing Zhou

- **High-Voltage MOSFET Model Valid for Device Optimization**  
Y. Oritsuki, T. Sakuda, N. Sadachika, M. Miyake, T. Kajiwara, H. Kikuchihara U. Feldmann, H.J. Mattausch, M. Miura-Mattausch, *Hiroshima University, JP*
- **Compare and Contrast HiSIM-LDMOS and BSIM based compact model of High Voltage MOSFETs for Analog Applications**  
A. Young, J. Hall, Z. Luo, Y. Xiao, D. Connerney, *Fairchild Semiconductor, US*
- **A Scalable POWER MOSFET Model with an Integrated Body-Diode Including Reverse Recovery**  
Z. Luo, J. Hall, Y. Xiao, A. Young, R. Carroll, D. Connerney, *Fairchild Semiconductor, US*
- **A PSpice Compact Model for Organic Field-Effect Transistors**  
C. Ucurum, R.M. Meixner, H. Goebel, *Helmut Schmidt University - University of the Federal Armed Forces Hamburg, DE*

## **WCM: Statistical/variation/numerical models**

Wed, 10:30am. Session chair: Henok Abebe

- **Compact Model Application to Statistical/Probabilistic Technology Variations**  
*X. Zhou, G. Zhu, M. Srikanth, R. Selvakumar, Y. Yan, W. Chandra, J. Zhang, S. Lin, C. Wei, Z. Chen, Nanyang Technological University, SG*
- **Elements of Statistical SPICE Models**  
*N. Lu, J. Watts, S.K. Springer, IBM, US*
- **PSP Model Equations Extension for Statistical Estimation of Leakage Current in Nanometer CMOS Technologies Considering Process Variations**  
*C. D'Agostino, P. Flatresse, E. Beigne, M. Belleville, STMicroelectronics, FR*

# WCM: RF/noise/capacitance models

Wed, 1:30pm. Session chair: Henok Abebe

- **RF Modeling of 45nm Low-Power CMOS Technology**  
J. Wang, H. Li, L-H Pan, U. Gogineni, R. Groves, B. Jagannathan, M-H Na, W. Tonti, R. Wachnik, *IBM Semiconductor Research and Development Center, US*
- **Compact Model of Low – Frequency Noise in Nanoscale Metal-Oxide-Semiconductor Field Effect Transistors**  
D.A. Miller, M.E. Jacob, L. Forbes, *Oregon State University, US*
- **1/f Noise Modeling at Low Temperature with the EKV3 Compact Model**  
P. Martin, G. Ghibaudo, *CEA, LETI, Minatec, FR*
- **1/f Noise Model for Double-Gate FinFET Biased in Weak Inversion**  
C-Q Wei, Y-Z Xiong, X. Zhou, *Nanyang Technological University, SG*
- **A Simple, Accurate Capacitance-Voltage Model of Undoped Silicon Nanowire MOSFETs**  
S. Lin, X. Zhou, G.H. See, G. Zhu, C. Wei, J. Zhang, Z. Chen, *Nanyang Technological University, SG*

## WCM: Parameter extraction/circuit design

Wed, 3:30am. Session chair: Xing Zhou

- **SPICE BSIM3 Model Parameters Extraction and Optimization for Low Temperature Application**  
*H. Abebe, V. Tyree, N.S. Cockerham, USC ISI/MOSIS, US*
- **An SOA Aware MOSFET Model for Highly Integrated, Analog Mixed-Signal Design Environments**  
*J. Hall, Z. Luo, Y. Xiao, A. Young, D. Connerney, Fairchild Semiconductor, US*
- **Automatically Generated and Experimentally Validated System-Level Model of a Microelectromechanical RF Switch**  
*M. Niessner, G. Schrag, G. Wachutka, J. Iannacci, B. Margesin, Munich University of Technology, DE*