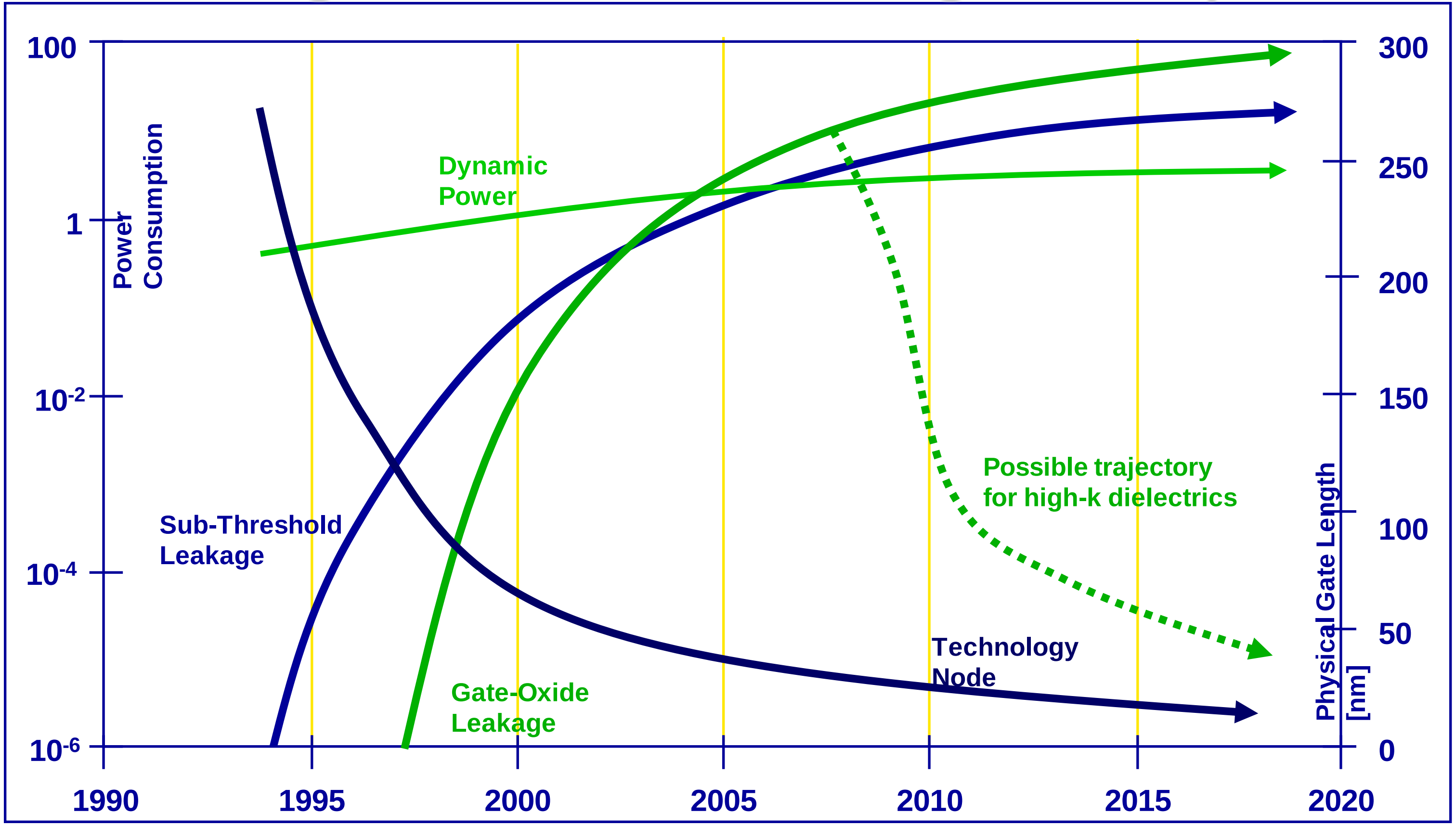
PSP Model Equation Extension for Statistical Estimation of Leakage Current in Nanometer CMOS Technologies Considering Process Variations

C. D’Agostino, P. Flatresse, E. Beigne, M. Belleville

Leakage trends

Subthreshold and gate **leakage dramatically increase** with each successive technology node

=> Leakage currents cannot be neglected anymore

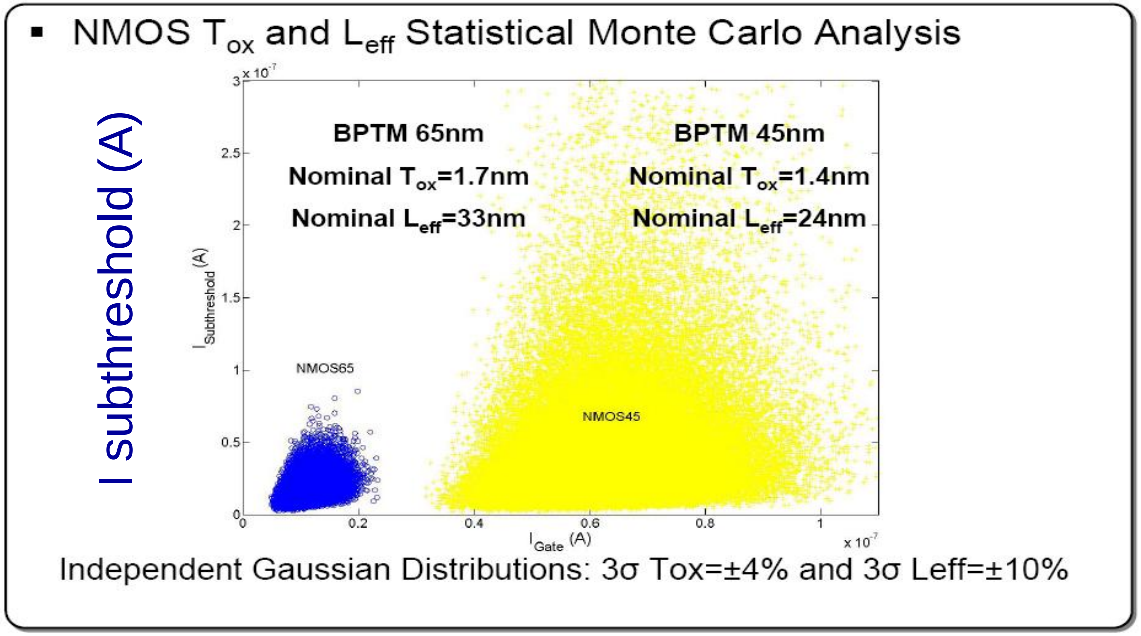


ISSCC 2008 - SoC Power-Reduction Techniques Tutorial – P. Urard

Computation Time

Direct **Monte-Carlo** (MC) simulation is computationally **too expensive** to estimate the statistical leakage distribution of **complex** circuits

=> MC simulations flow not applicable to nowadays ICs design flow



- NMOS T_{ox} and L_{eff} Statistical Monte Carlo Analysis

Independent Gaussian Distributions: 3σ Tox=±4% and 3σ Leff=±10%

ISSCC 2008 - SoC Power-Reduction Techniques Tutorial – P. Urard

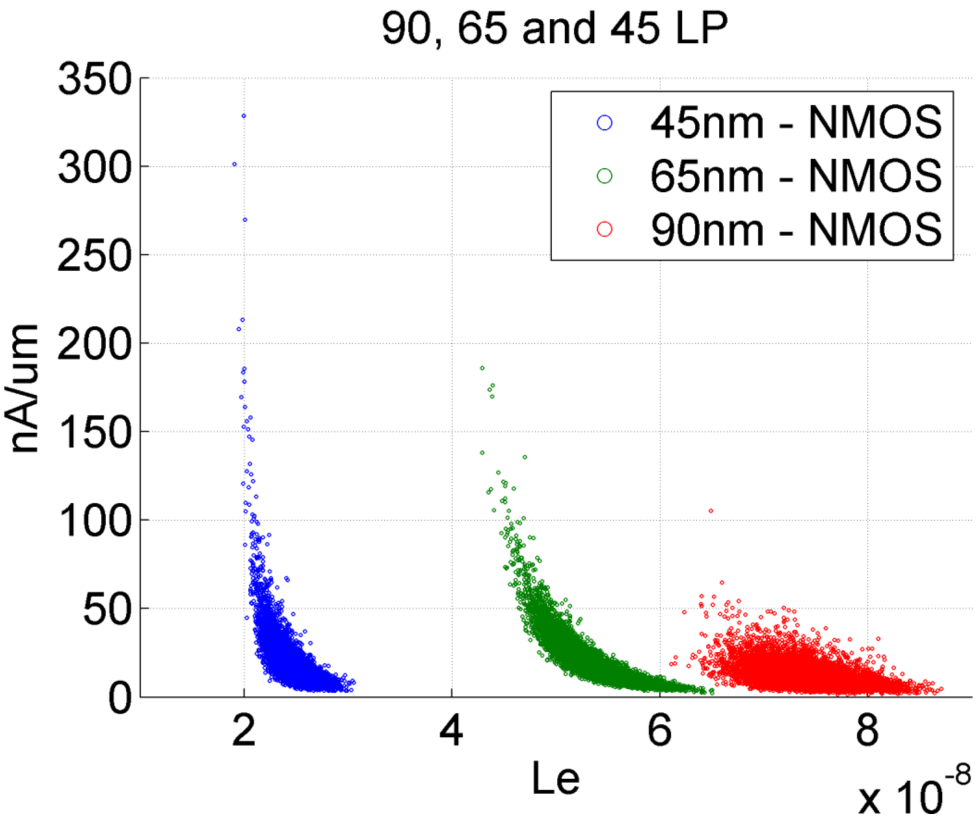
State of the art **statistical leakage analysis** methodology are based on:

- approximated PSP or BSIM models
- new transistor models

Variability Issues

Process parameter variations make devices and interconnects appear as **statistical variables**

=> Classic corner based approach is too pessimistic

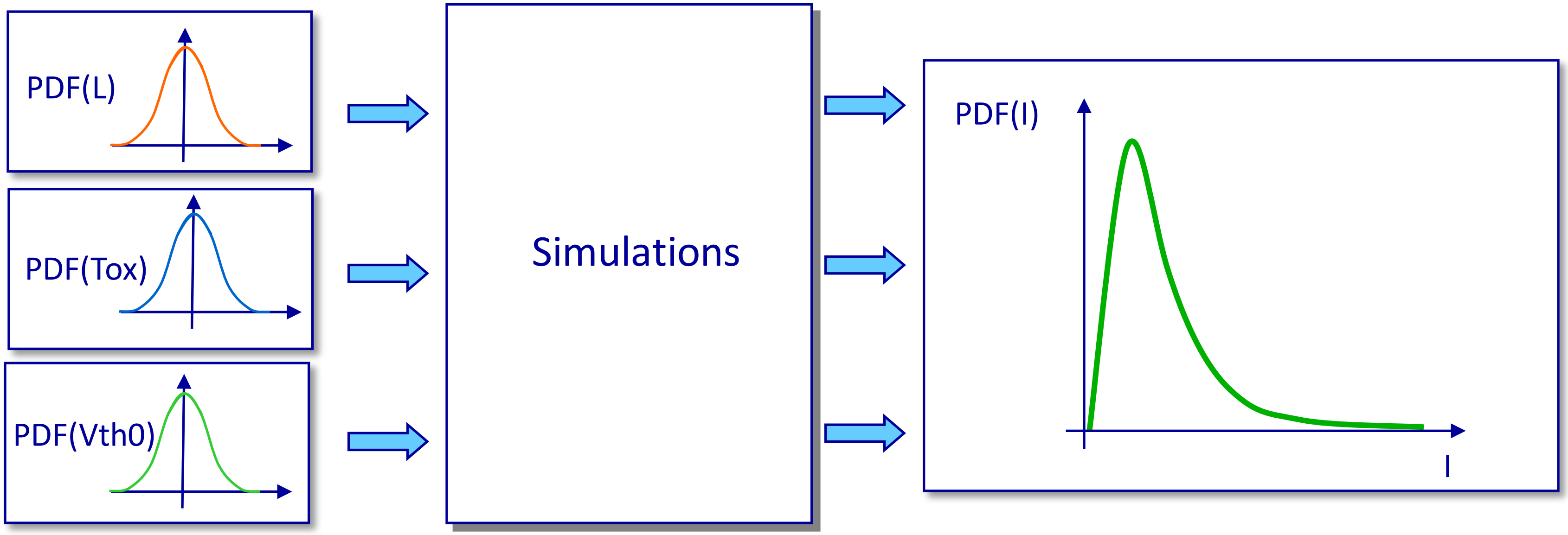


Outline

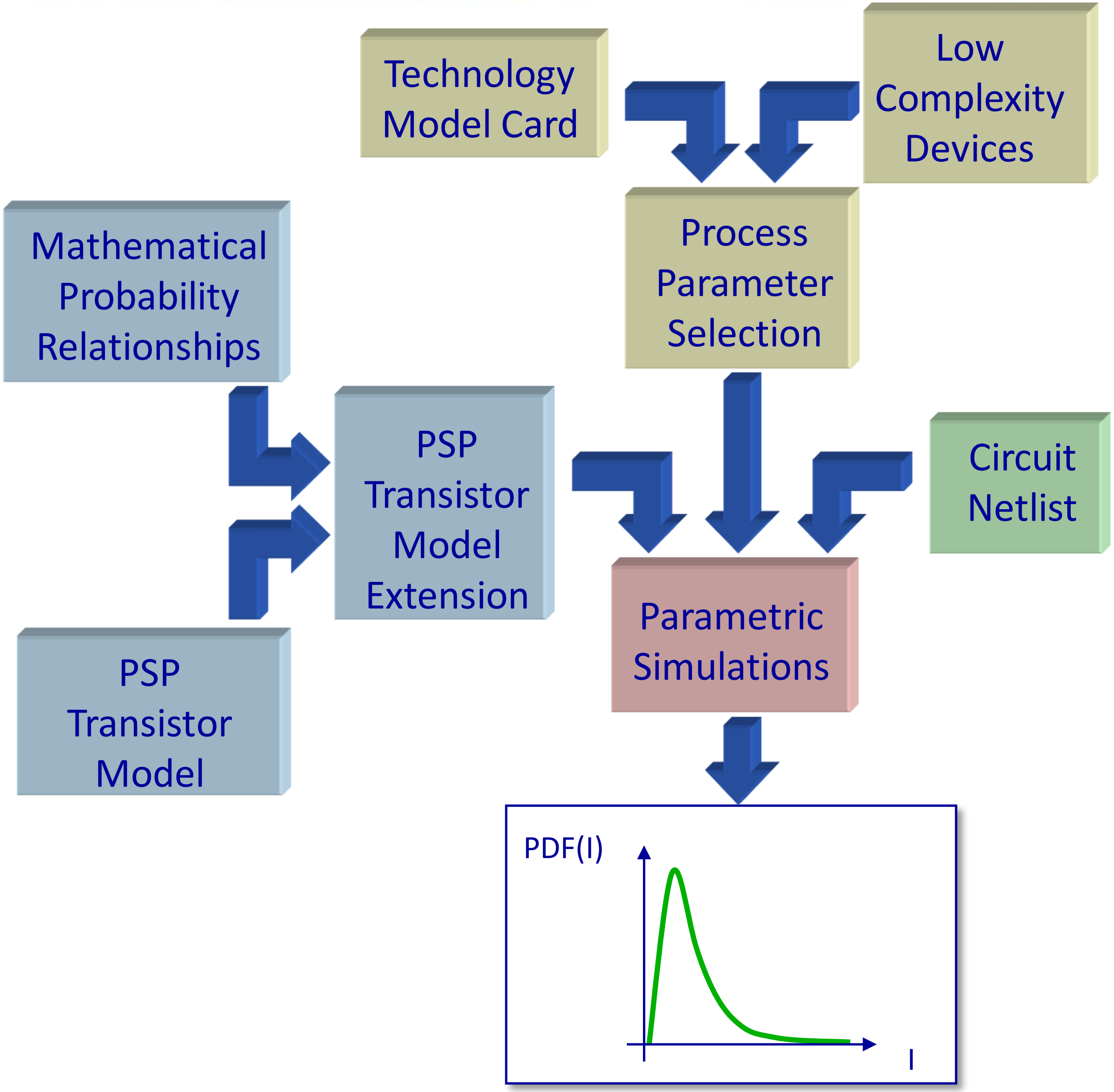
- Objectives of this work
- General statistical leakage analysis overview
- Process parameter selection
- PSP model extension: mathematical background
- PSP model extension: implementation
- Simulation Strategy
- Results
- Conclusions

Objective of this work

Compute the **analytical expression** of the Probability Density Function (PDF) of leakage current considering the statistical variations of the **technological parameters**



General methodology overview



Technology Model Card

Low Complexity Devices

Process Parameter Selection

Mathematical Probability Relationships

PSP Transistor Model Extension

Circuit Netlist

Parametric Simulations

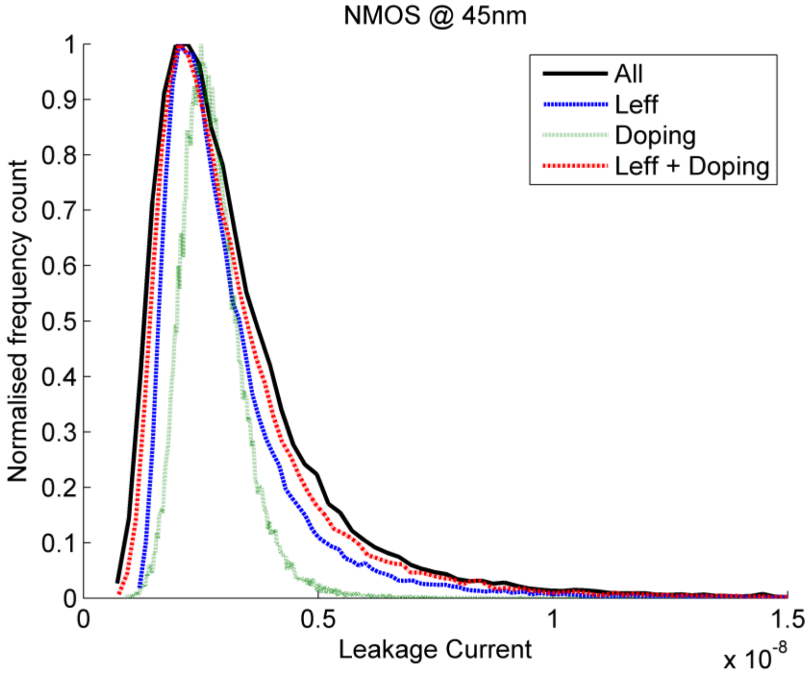
PSP Transistor Model

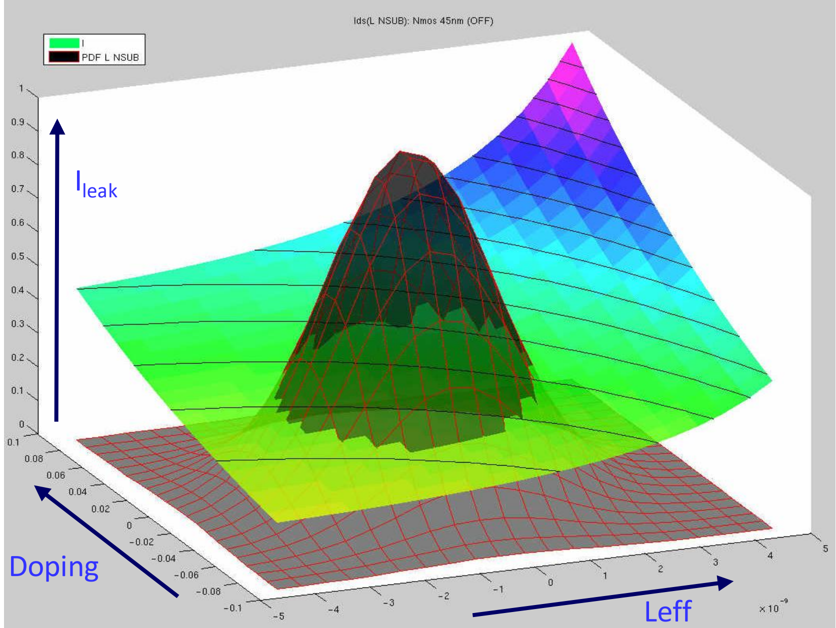
Process Parameter Selection

Each leakage contribution in a CMOS device depends on **more than one** process parameter

The impact of process parameter variations on the leakage PDF **is different** for each technology node

In 45nm to estimate the PDF of the leakage current it is necessary to consider at least the **variations of the gate length** and the **variations of the dopant concentration**





PSP Model Extension: Mathematical Background (1)

Considering L_{gate} as varying process parameter, we need:

Function **$h(L_{gate})$** => $I_{leak}(L_{gate})$

Function **$h'(L_{gate})$** => First derivative of $I_{leak}(L_{gate})$

Function **$g(I_{leak})$** => $L_{gate}(I_{leak}) = f^{-1}(h)$

Function **$PDF(L_{gate})$** => f_x (Generally Gaussian)

We get:

$$PDF(I_{leak}) = f_y = \frac{f_x(g(I_{leak}))}{h'(L_{gate})}$$

Problem:

the function **Ileak(Lgate)** used in PSP model **is not** analytically invertible!

Solution:

use the **intrinsic** calculations of SPICE simulator engine to express the PDF(I) directly as **function of Lgate**

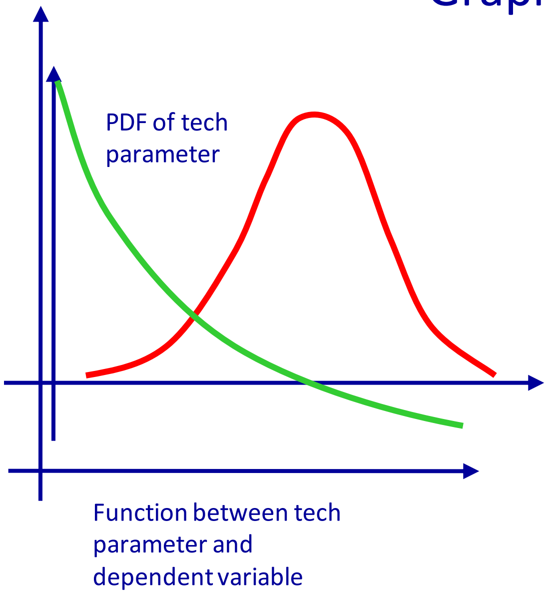
$$PDF(I_{leak}) = f_y = \frac{f_x(L_{gate})}{h'(L_{gate})}$$

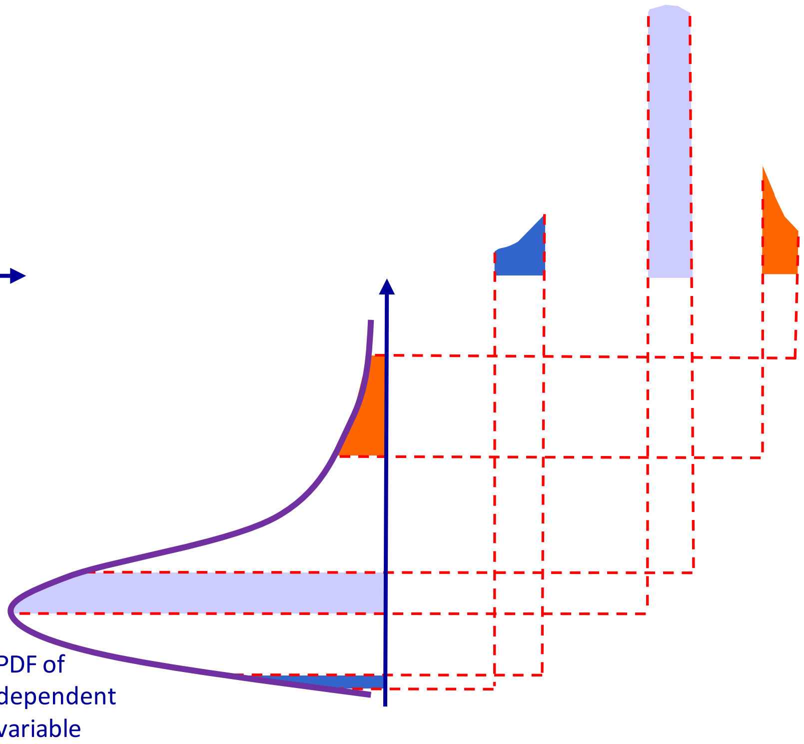
PSP Model Extension: Mathematical Background (2)

Mathematical expression

$$PDF(I) = \frac{PDF(TechParam)}{\frac{dI}{dTechParam}}$$

Graphical Interpretation





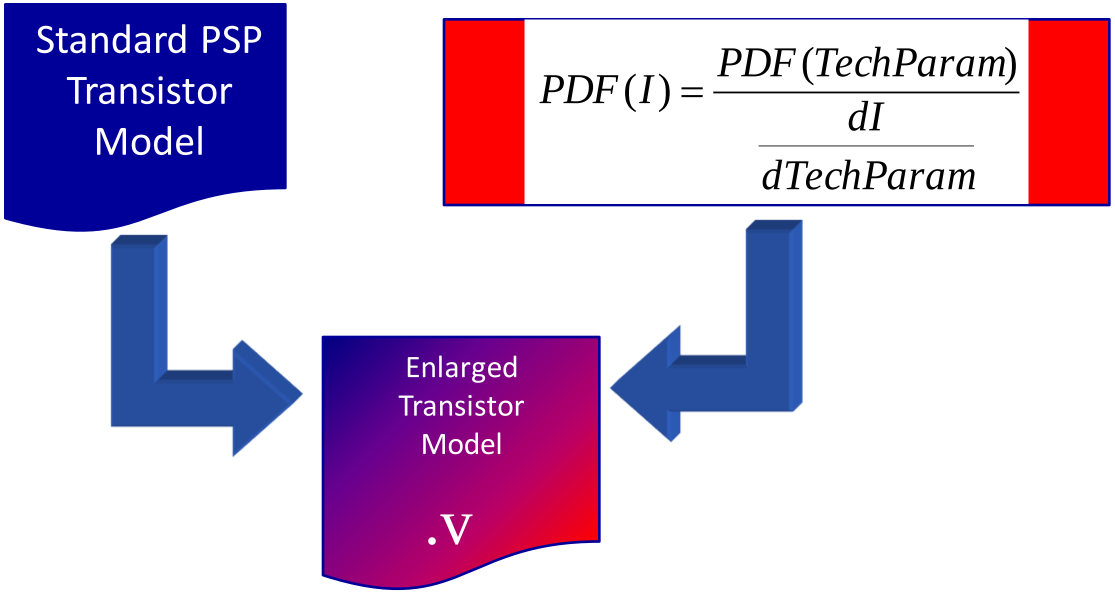
PSP Model Extension: implementation (1)

In the current implementation is used the PSP model coded in **verilog-A**

In the extended PSP transistor model **have been included**:

- The **derivatives** of each leakage current respect to the selected process parameters
- The **PDFs** of the selected process parameter (defined in the technology model card)

All the other equations remain **untouched**



Standard PSP Transistor Model

$$PDF(I) = \frac{PDF(TechParam)}{\frac{dI}{dTechParam}}$$

Enlarged Transistor Model

.V

PSP Model Extension: implementation (2)

Two virtual pins are added to the transistor model in order to have directly the PDF value of the leakage current as SPICE **simulation output**

Transistor node definition:

```
...
   inout      D, G, S, B, PDF_I_LEFF, PDF_I_LEFF;
   electrical D;
   electrical G;
   electrical S;
   electrical B;
   electrical PDF_I_LEFF;
   electrical PDF_I_NSUB;
...
```

The **PDFs equations** of gate length and dopant concentration (defined in the technology model cards) are coded in the **Verilog-A** PSP model files

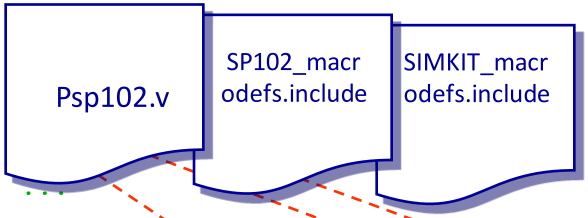
Example of PDF of gate length and doping concentration assuming Gaussian distributions:

```
...
PDF_L = (1/(sigma_dl *sqrt(2*`PI)))*exp(-(pow((LVARO-mu_dl),2))/(2*sigma_dl*sigma_dl));
...
PDF_NSUB = (1/(sigma_dnsub *sqrt(2*`PI)))*exp(-(pow((NSUBO-mu_dnsub),2))/(2*sigma_dnsub*sigma_dnsub));
...
```

PSP Model Extension: implementation (3)

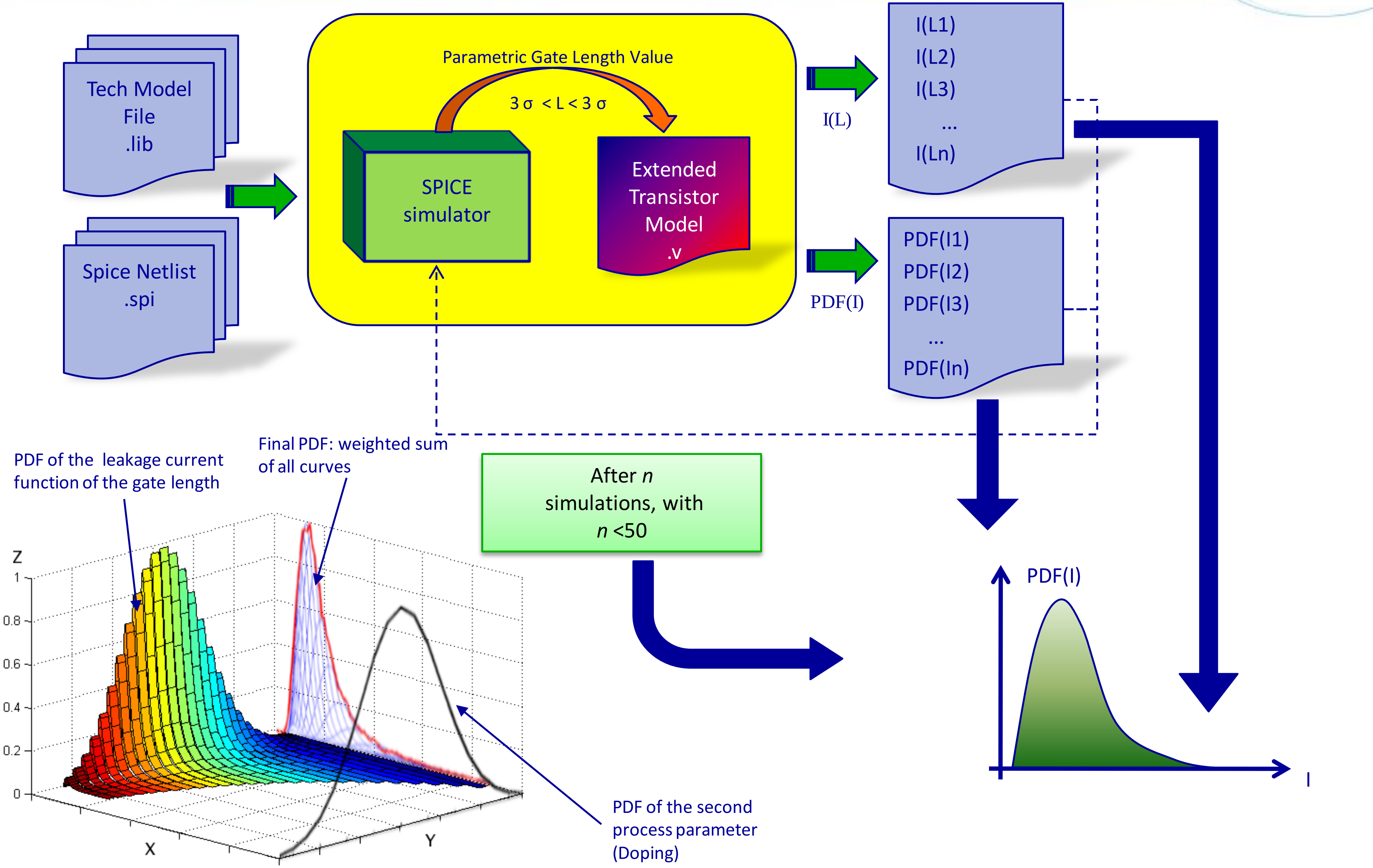
Analytical derivative for each leakage current, respect to the gate length and dopant concentration, are coded in the **Verilog-A** PSP model files

Example of Ids derivation respect to the variations in gate length



```
  ...
  ...

deriv_BET_i_dl = FACTUO_i * deriv_BET_i_dl * CoxPrime * tf_bet + FACTUO_i * BET_i * CoxPrime * deriv_tf_bet_dl ;

  ...
  ...

deriv_MULT_i_dl =0;

  ...
  ...

Ids =  BET_i * (FdL * qim1 * dps * Gvsatinv);
deriv_Ids_dl = deriv_BET_i_dl * (FdL * qim1 * dps * Gvsatinv)+ BET_i * (deriv_FdL_dl * qim1 * dps * Gvsatinv)+
               BET_i * (FdL * deriv_qim1_dl * dps * Gvsatinv)+ BET_i * (FdL * qim1 * deriv_dps_dl * Gvsatinv)+
               BET_i * (FdL * qim1 * dps * deriv_Gvsatinv_dl);

   ...
   ...

 Idse = MULT_i * Ids;
 deriv_Idse_dl = MULT_i * deriv_Ids_dl + deriv_MULT_i_dl * Ids ;
```

Simulation Strategy



Tech Model File .lib

Spice Netlist .spi

Parametric Gate Length Value

$3\sigma < L < 3\sigma$

SPICE simulator

Extended Transistor Model .v

I(L)

I(L1)
I(L2)
I(L3)
…
I(Ln)

PDF(I)

PDF(I1)
PDF(I2)
PDF(I3)
…
PDF(In)

After *n* simulations, with *n* <50

PDF of the leakage current function of the gate length

Final PDF: weighted sum of all curves

PDF of the second process parameter (Doping)

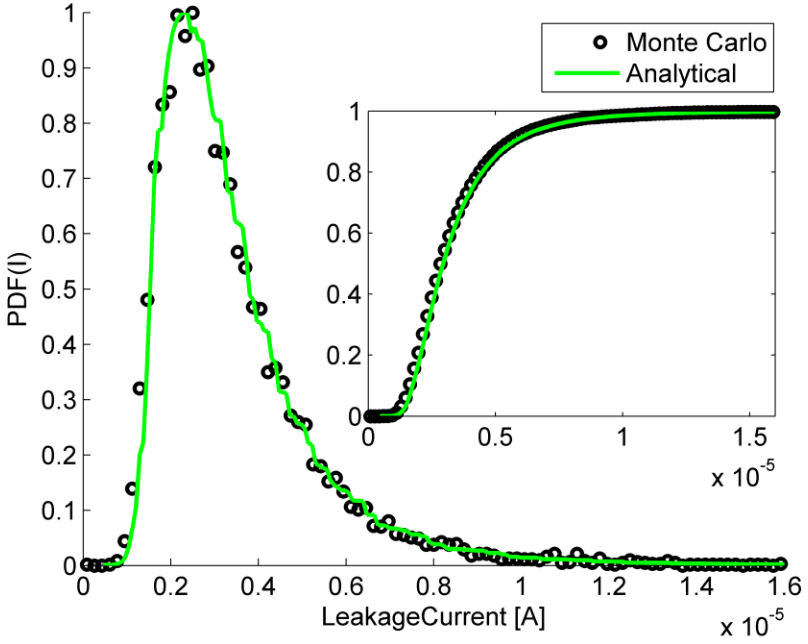
Results

At **45nm** technology node, **comparisons** with extensive Monte-Carlo on simulations show the **accuracy** and **saving** (in term of computational time) of the proposed approach

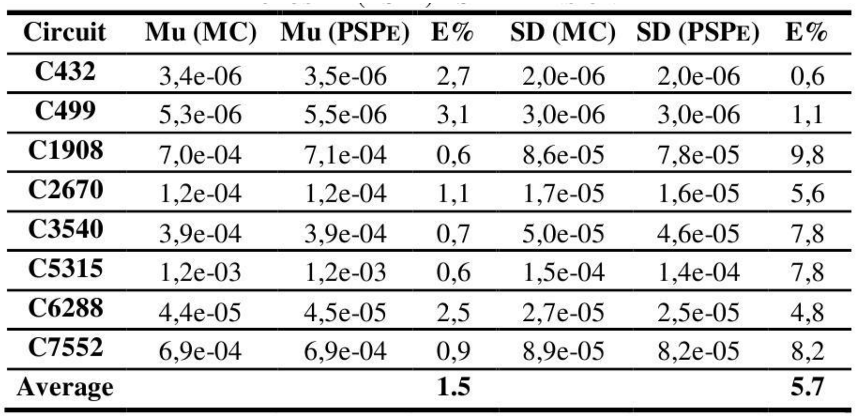
Simple two logic gate statistical leakage example (@45 nm):

○ 10000 MC Simulations

— 500 Parametric Simulation



Medium complexity logic circuits (ISCAS):



Circuit	Mu (MC)	Mu (PSPE)	E%	SD (MC)	SD (PSPE)	E%
C432	3,4e-06	3,5e-06	2,7	2,0e-06	2,0e-06	0,6
C499	5,3e-06	5,5e-06	3,1	3,0e-06	3,0e-06	1,1
C1908	7,0e-04	7,1e-04	0,6	8,6e-05	7,8e-05	9,8
C2670	1,2e-04	1,2e-04	1,1	1,7e-05	1,6e-05	5,6
C3540	3,9e-04	3,9e-04	0,7	5,0e-05	4,6e-05	7,8
C5315	1,2e-03	1,2e-03	0,6	1,5e-04	1,4e-04	7,8
C6288	4,4e-05	4,5e-05	2,5	2,7e-05	2,5e-05	4,8
C7552	6,9e-04	6,9e-04	0,9	8,9e-05	8,2e-05	8,2
Average			1.5			5.7

Accuracy can be easily **compromised** with **simulation time** selecting the appropriate number of parametric simulations

Conclusions

The proposed methodology:

- Predict median, standard deviation, and the shape of the PDF of the leakage current
- Use the complete PSP transistor model (no need of extra empirical fitting parameters)
- Consider variations of several process parameters at the same time
- Currently is implemented in verilog-A
- Has been verified by means of extensive Monte-Carlo simulations @ 45nm tech node

Thank You!

email: carmelo.dagostino@st.com