

The World Leader in High Performance Signal Processing Solutions



Source/Drain Junction Partition in MOS Snapback Modeling for ESD Simulation

**Yuanzhong (Paul) Zhou,
Jean-Jacques Hajjar**

**Analog Devices Inc.
Wilmington, MA, USA**

WCM 2008, June 3-4, Boston





Outline

- ◆ **Motivation**
- ◆ **Compact Modeling for ESD Application**
 - On-Chip ESD Protection Scheme
 - Brief Review on Compact ESD Modeling for Snapback
 - Macro Model using Advanced MOS and BJT Models
- ◆ **Enhanced Model with Junction Partition**
 - Discrepancies in Existing Model
 - Macro Model with Junction Partition
 - Simulation using New Model
- ◆ **Conclusion**

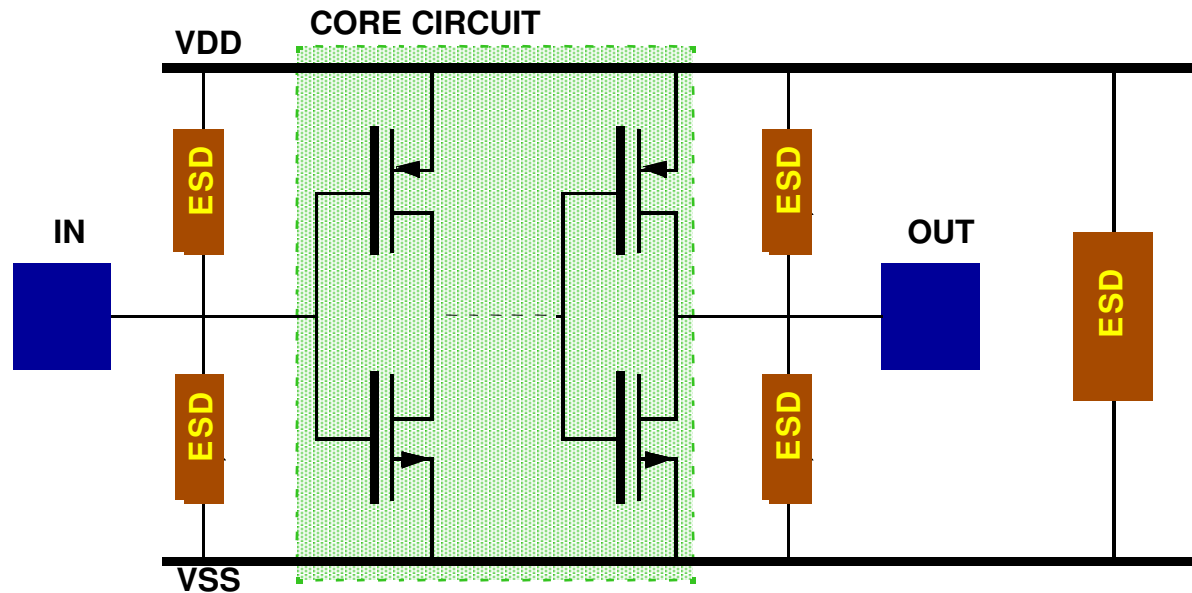


Motivation

- ◆ **Why SPICE-type ESD simulation?**
 - **ESD Protection Cell Design Aid**
 - **ESD Performance Prediction Prior to Silicon**
 - **ESD Failure/Weakness Analysis**

- ◆ **Prominent Modeling Challenges:**
 - **Devices operate beyond process rated current/voltage**
 - **ESD-capable Compact Model**
 - **Practical SPICE Model**

On-Chip ESD Protection Schemes



During ESD events, ESD protection

- shunts high current discharges away from the core circuitry
- clamps pad voltage to a safe level

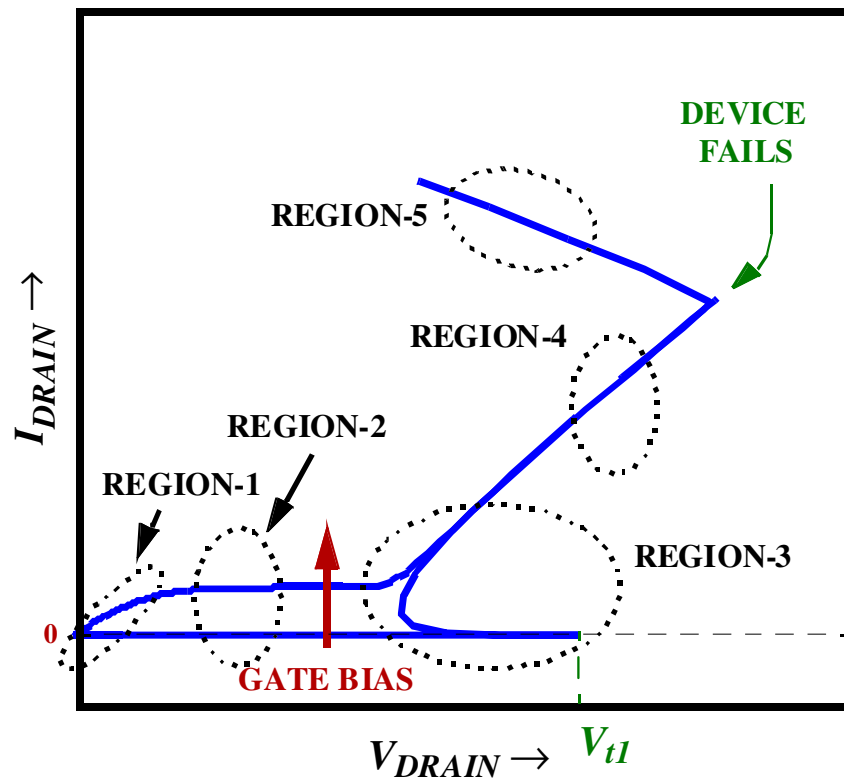
Snapback in ESD Devices

◆ Operating I-V Regions of MOS Devices

- 1) Linear Region
- 2) Saturation Region
- 3) Avalanche Region
- 4) Snapback Region
- 5) Failure Region

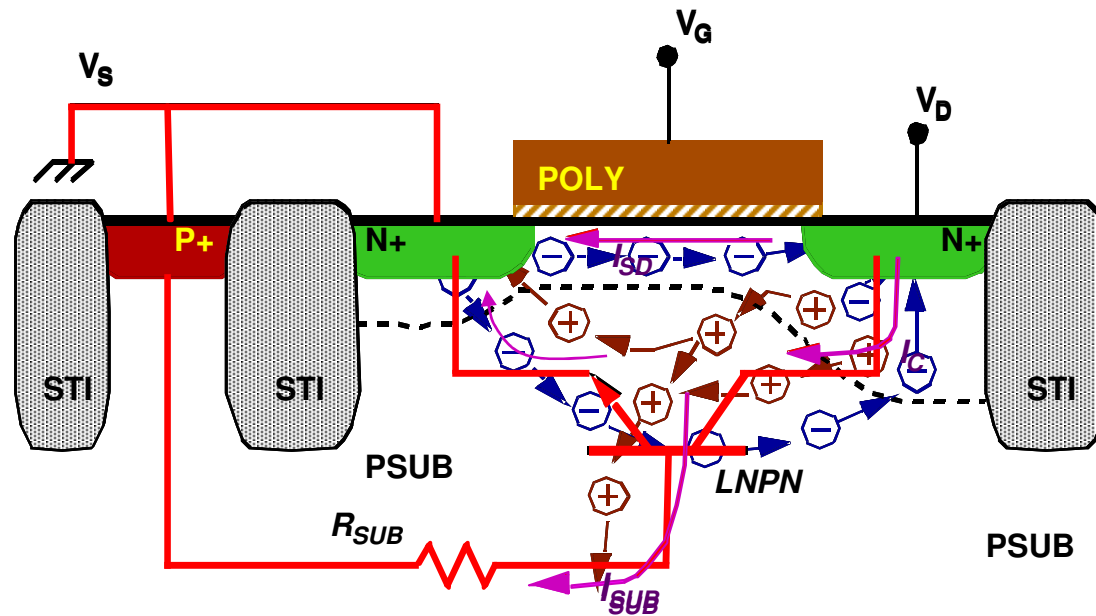
◆ V_{t1} represents the “snapback effect” trigger voltage

◆ Devices (MOS) operating in “snapback” mode carries more current per unit width



Snapback in MOS Devices (cont.)

Snapback Effect in MOS is due to turning on of the Parasitic BJT, triggered by the substrate current (I_{SUB}).

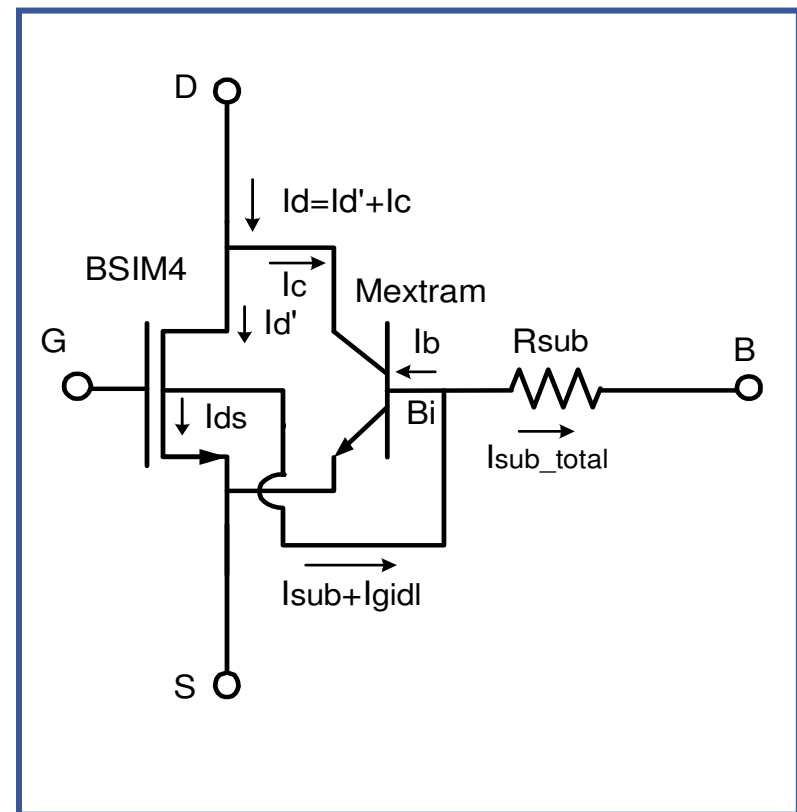


Critical Effects in Snapback Modeling

- ◆ Voltage drop across Base/Emitter junction of parasitic NPN
- ◆ Substrate current as function of V_{DS} , V_{GS} and V_{BS}
 - Due to impact ionization in Drain/Body depletion layer
 - Multiplication factor is different before and after snapback
 - Displacement current (dV/dt) through Drain/Body junction
 - Gate induced drain leakage (GIDL)
- ◆ The base transit time of the parasitic NPN
- ◆ Snapback models must have:
 - Main MOS
 - Parasitic BJT
 - Substrate Resistor
 - Avalanche Current Source

Macro Model for MOS Snapback

- ◆ New approach eliminates the current source. [1]
- ◆ Model Consists of Standard Components only.
- ◆ Intrinsically includes all major effects outlined.



[1] Zhou et al, ISQED 2005

Key Effects in the Macro Model

Summary

- ◆ Current sources for avalanche and GIDL are intrinsically built into MOS and BJT models.

$$I_{GEN} = I_{AVL} + I_{SUB} + I_{GIDL}$$

- ◆ Decoupled multiplication factors for BJT and MOS are included in I_{AVL} and I_{SUB} respectively.
- ◆ The dV/dt effect is modeled by C/B junction capacitance of BJT.
- ◆ The transit time of the BJT is included in the BJT model.

Discrepancies in Existing Models

- ◆ Fail to accurately model the impedance for negative V_{DS}
- ◆ Different capacitance values for Base/Collector junction from CV measurement and transmission line pulse (TLP) measurement data
- ◆ Different current gain (beta) of the BJT from DC measurement and TLP data

Enhanced Model by Junction Partition

- ◆ Add S/B D/B Junction Diodes to Macro Model

- ◆ Substrate current becomes

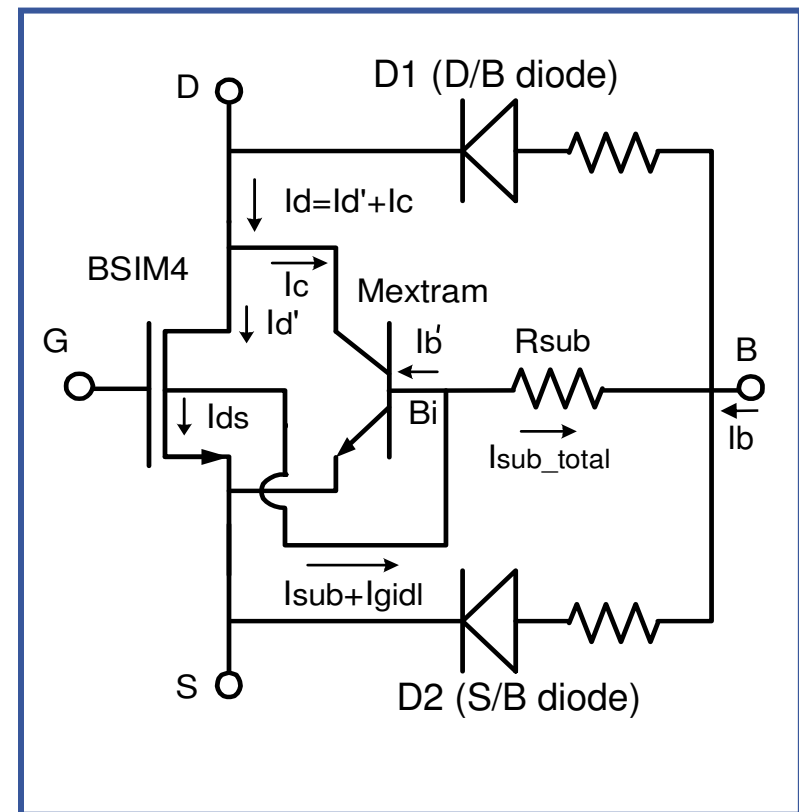
$$I_{gen} = I_{sub} + I_{gidl} + I_{avl} + I_{dio1}$$

- ◆ D/B Junction Capacitance

$$C_{DB} = CJC_{BJT} + CJ_{D1}$$

- ◆ Total base terminal current when the BJT in forward Gummel configuration

$$I_b = I_b' + I_{dio2}$$

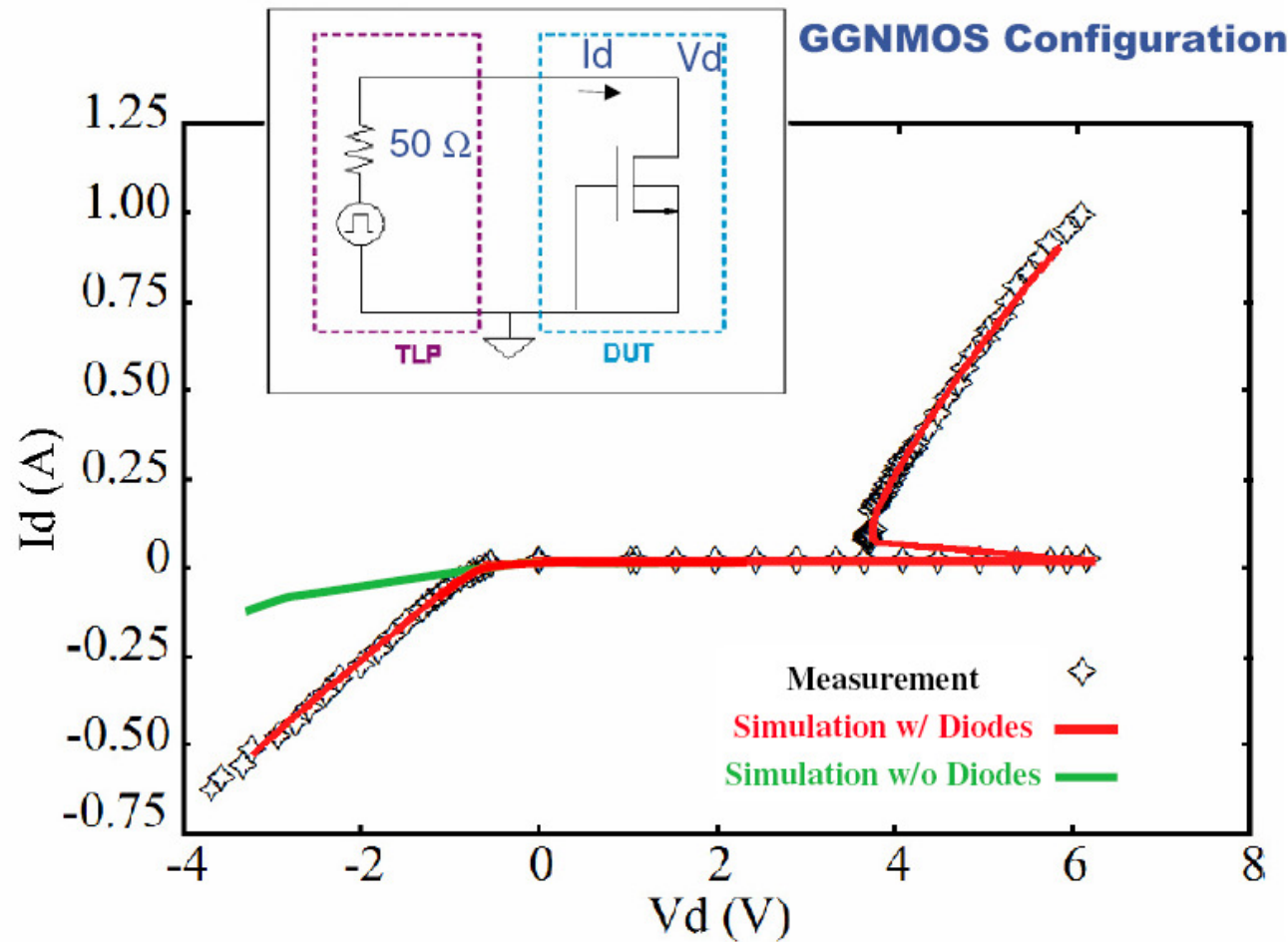


Model Extraction Flow

- ◆ Extract the MOS and BJT models for DC and AC operation using standard practice
- ◆ Obtain substrate resistance R_{SUB} , BJT parameters C_{JC} and B_F from snapback characteristics
- ◆ Determine diode parameters from IV curve for $V_{DS} < 0$ and total junction capacitance.

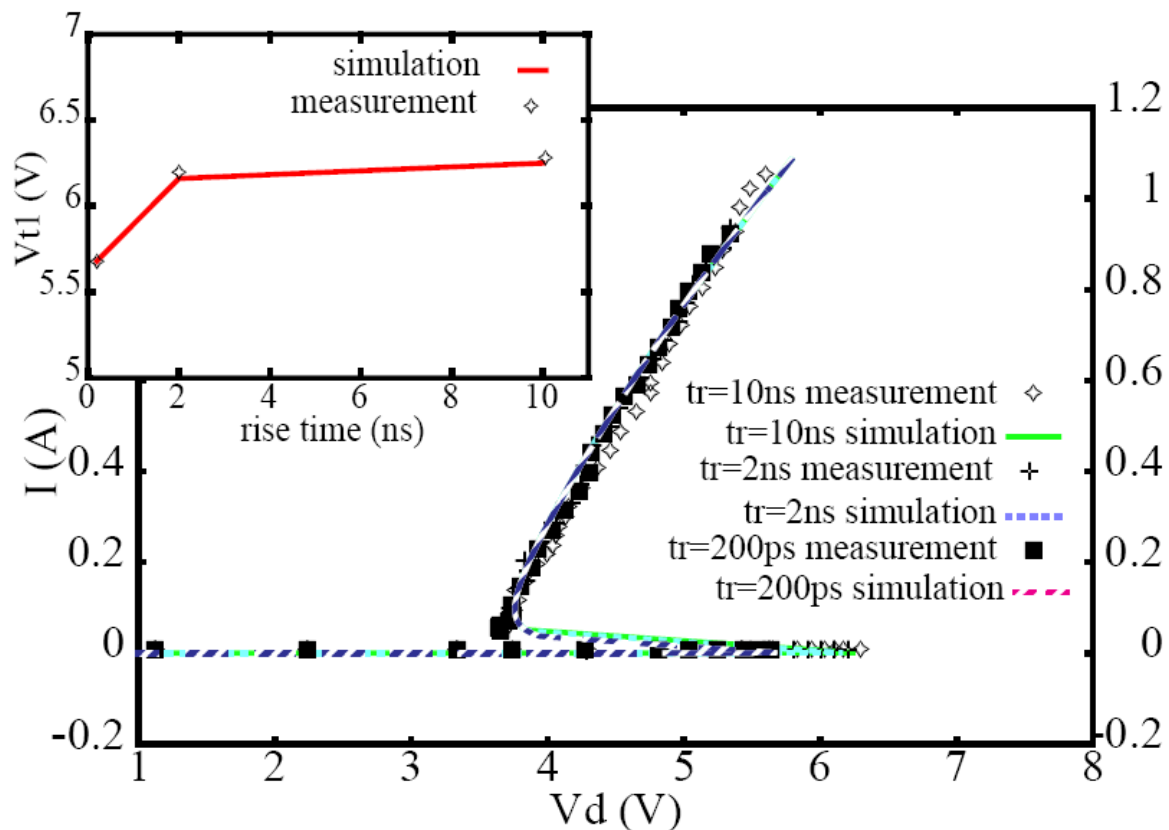
Simulation Results vs. TLP Measurement

-- A ggNMOS device



Simulation Results vs. TLP Measurement

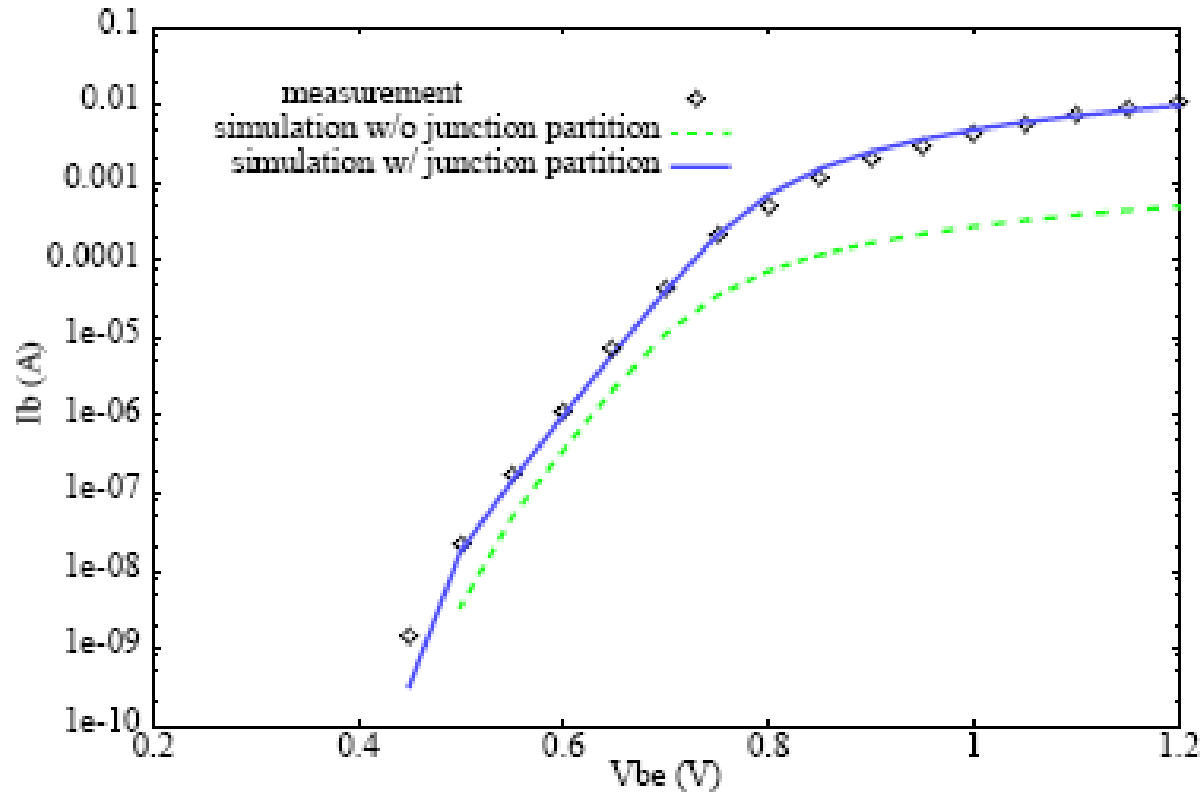
--Snapback curves of a ggNMOS device for different rise times



$$C_{JC_{BJT}}/C_{DB} \approx 0.9$$

SPICE Simulation Results

-- Base current in forward Gummel plot for the parasitic BJT



$$I_{S_{BJT}} / (I_{S_{BJT}} + I_{S_{DIO}}) \cong 0.6$$

Conclusion

- ◆ Junction partition in MOS snapback model has been discussed using a new macro model approach
- ◆ Enhanced compact model retains the advantages in the original approach
 - Uses industry standard models
 - Simple implementation
 - High simulation speed
 - Wide accessibility
 - Fewer convergence issues
- ◆ New model offers significant improvement
 - Valid for both positive and negative V_{DS} stresses
 - Consistent total drain capacitance
 - Accurate base current for the parasitic BJT