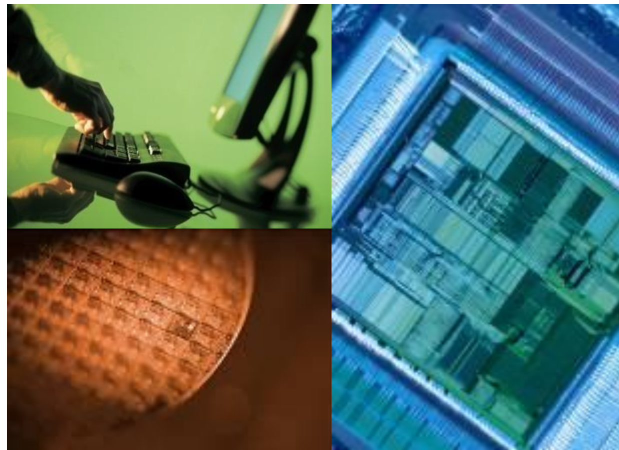
Process Aware Compact Model Parameter Extraction for 45 nm Process Flow



A. P. Karmarkar, V. K. Dasarapu,
A. R. Saha, G. Braun,
S. Krishnamurthy and X.-W. Lin

Synopsys, Inc.
700 East Middlefield Road,
Mountain View, CA, USA.

SYNOPSYS®
Predictable Success

Motivation

- Sub 100-nm designs are highly sensitive to process variations
- Parametric variation is a significant cause of yield loss
- Conventional modeling cannot adequately capture the process variability impact
- Process-aware SPICE models capture the entire process space and allow for process and design optimization
- These models provide better control over the power and performance constraints, leading to more robust designs

Outline

- Process variability and impact of process variability
- Process aware-spice models
- The 45 nm process flow
- Process aware parameter extraction for the 45 nm process
- Circuit simulation results
- Summary and conclusions

SYNOPSYS®
Predictable Success

Outline

- **Process variability and impact of process variability**
- Process aware-spice models
- The 45 nm process flow
- Process aware parameter extraction for the 45 nm process
- Circuit simulation results
- Summary and conclusions

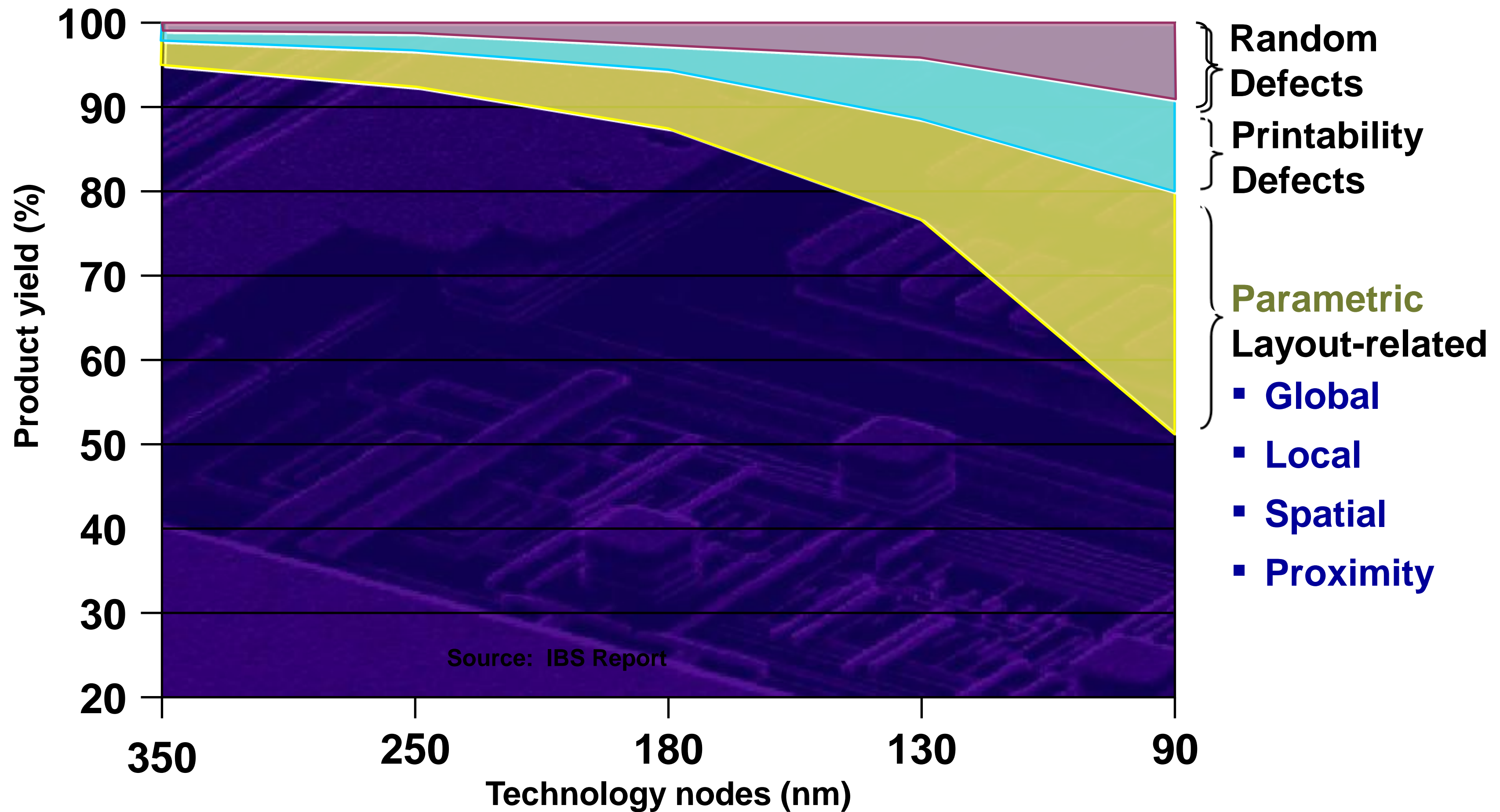
© 2008 Synopsys, Inc. (4)

Designing at sub-100 nm: A new paradigm

- Designs are highly sensitive to process variations
- Design intent may not be manufacturable
- Systematic variability dominates yield
  - Optical proximity effects
  - Stress proximity effects
  - CMP effects
- Symptom: Explosion of Design Rules
  - Restrictive Design Rules
  - Manufacturing Recommended Rules

SYNOPSYS®
Predictable Success

Yield loss trend



Parametric variation is a major contributor to yield loss!!

SYNOPSYS®
Predictable Success

Outline

- Process variability and impact of process variability
- **Process aware-spice models**
- The 45 nm process flow
- Process aware parameter extraction for the 45 nm process
- Circuit simulation results
- Summary and conclusions

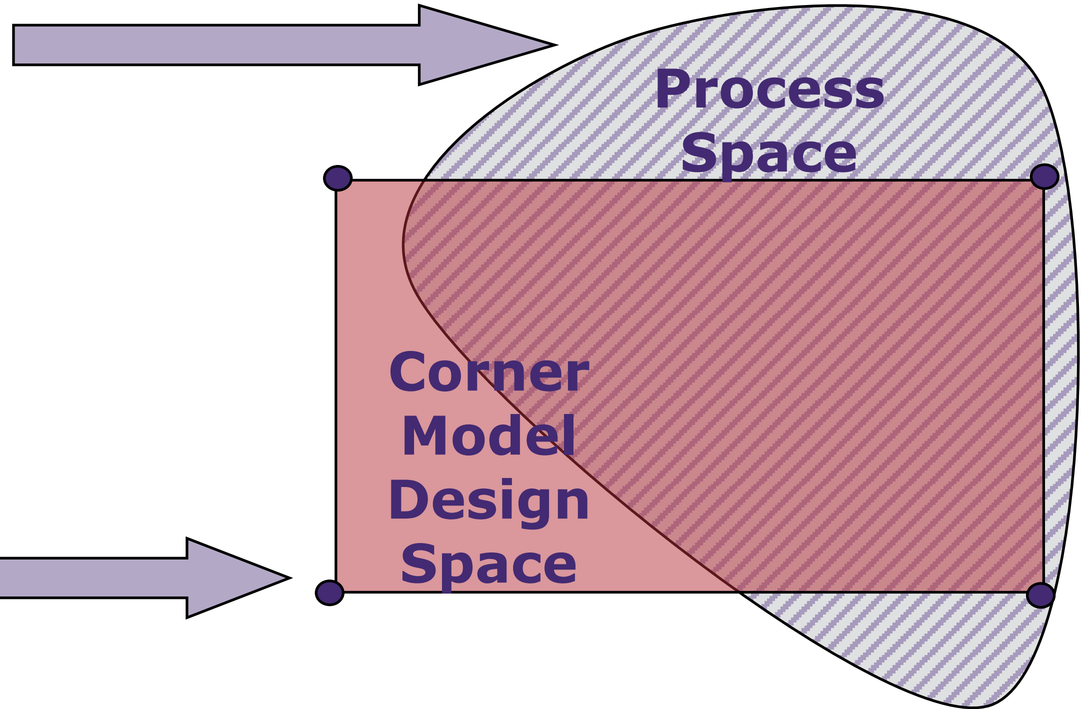
© 2008 Synopsys, Inc.

SYNOPSYS®
Predictable Success

Design Optimization Challenges

Why miss this region?

Why waste time to optimize for this corner ?



SYNOPSYS®
Predictable Success

Comparison of various modeling approaches

Worst Case Corner Model

Does not capture complex process

Statistical Models

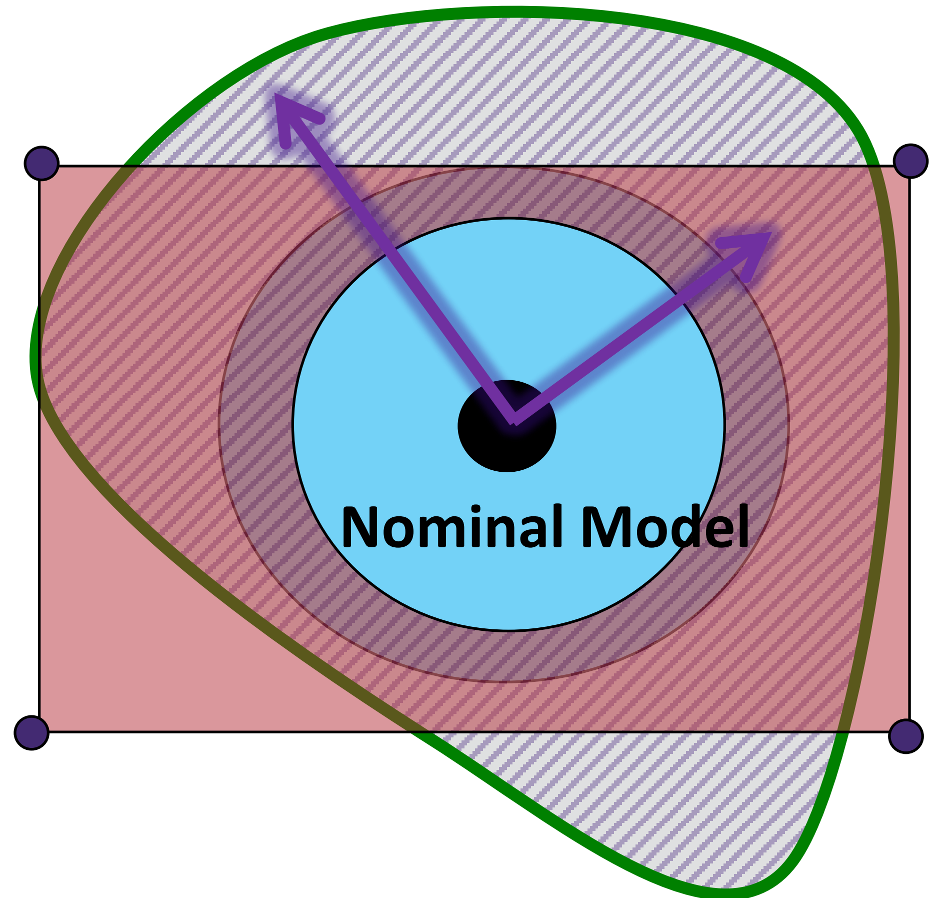
Does not fully capture the process

PCA Models

Converts process variation to abstract variation

Process Aware Model

Captures the actual process variations



SYNOPSYS®
Predictable Success

Process aware SPICE model

- It is a deterministic model
- Systematic and random process variations can be modeled
- Process Parameters
  - Measurable, adjustable and statistically independent
  - Monitored and recorded as part of on-going manufacturing process
  - {Pi} are NOT fitting parameters!
- Improves the understanding of the process variability impact design
- Allows desensitization of design to process variations and design specific process centering
- Allows for performing intelligent splits to find sweet spot

© 2008 Synopsys, Inc. (10)

Outline

- Process variability and impact of process variability
- Process aware-spice models
- **The 45 nm process flow**
- Process aware parameter extraction for the 45 nm process
- Circuit simulation results
- Summary and conclusions

© 2008 Synopsys, Inc.

SYNOPSYS®
Predictable Success

45 nm CMOS process flow

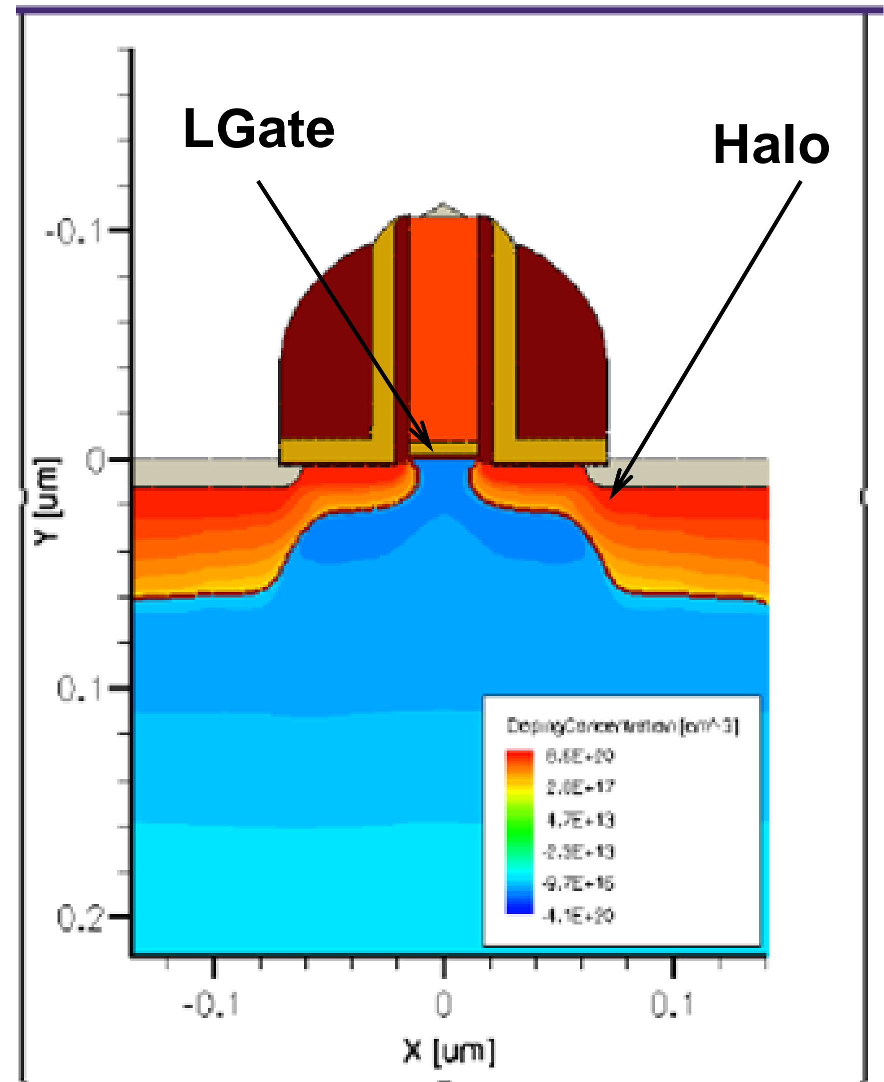
- **Reference flow based on ITRS 2006 ("Roadmap") targets for high-performance CMOS**
- **Full flow simulation illustrating advanced TCAD usage**

•Parameter	•Specification
•Source/drain (S/D) Junction Depth (Xj)	•15 nm
•Effective channel length	•0.5*Lgate
•Ion	•1.8 mA/µm
•Ioff	•100 nA/µm
•Wafer/Channel orientation	•100/110
•Stress memorization technique (SMT) (NMOS only)	•1.0 GPa (compressive)
•Channel stress NMOS/PMOS	•1-2 GPa (tensile) / 2–3 GPa (compressive)
•V_{tlin} short/long	•0.35 V/0.2 V
•V_{tsat} short/long	•0.18 V/0.2 V
•V_{supply}	•1 V

© 2008 Synopsys, Inc. (12)

45 nm CMOS process flow

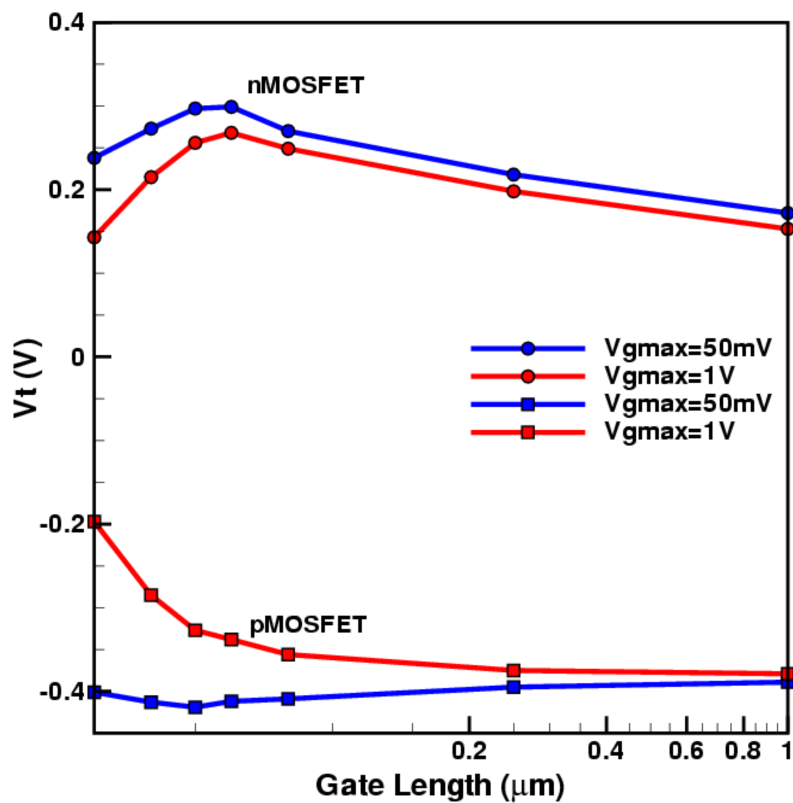
- STI
- Well Formation
- Gate Oxidation
- High-k Deposition
- Poly Deposition and Etch
  - SMT (nMOS only)
- Poly Reoxidation
- Offset Spacer
- HALO Implantation
- SD-Ext Implantation
- Sidewall Spacer
  - SiGe Pocket (pMOS only)
- HDD Implantation
- Laser Annealing
- Contact Silicidation
- Stress Liner



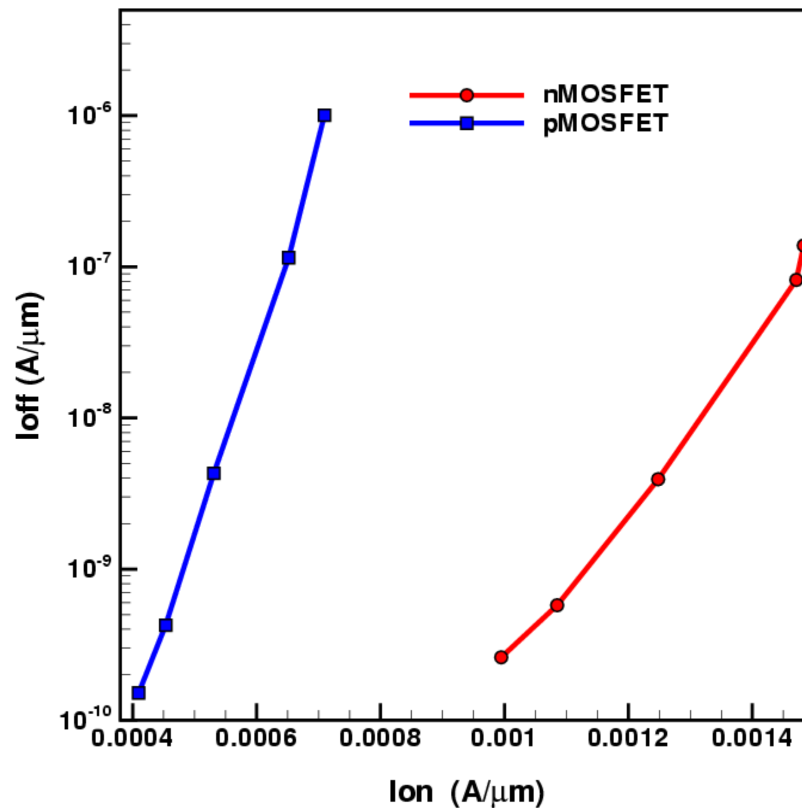
SYNOPSYS®
Predictable Success

Electrical results

V_t Roll-Off



I_{on}-I_{off}



© 2008 Synopsys, Inc. (14)

Outline

- Process variability and impact of process variability
- Process aware-spice models
- The 45 nm process flow
- **Process aware parameter extraction for the 45 nm process**
- Circuit simulation results
- Summary and conclusions

© 2008 Synopsys, Inc.

SYNOPSYS®
Predictable Success

Parameter Selection

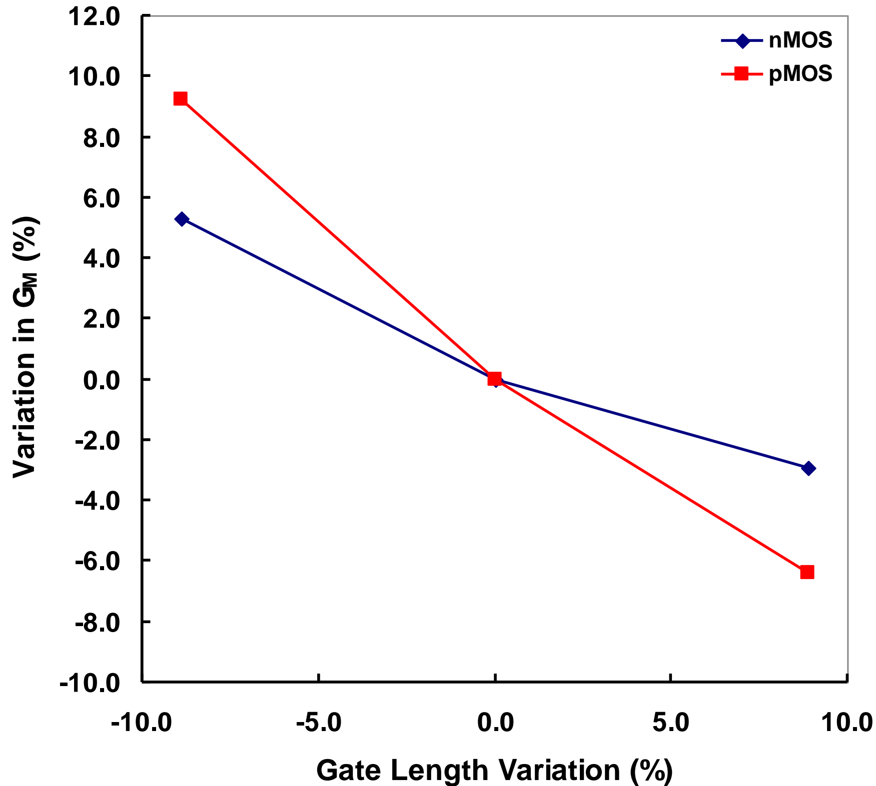
- Process meters that have the greatest impact on device characteristics are selected
  - Geometric parameters have the largest impact
- Gate oxide thickness is not varied as the gate insulator is a combination of SiO_2 and HfO_2
  - Equivalent oxide thickness (EOT): 0.812 nm
- Variation Details
  - Gate length varied from 41 nm to 49 nm
  - Halo Dose variation of ±10%
  - Halo Energy variation of ± 10%
  - Gate taper angle varied from 0° to 8°

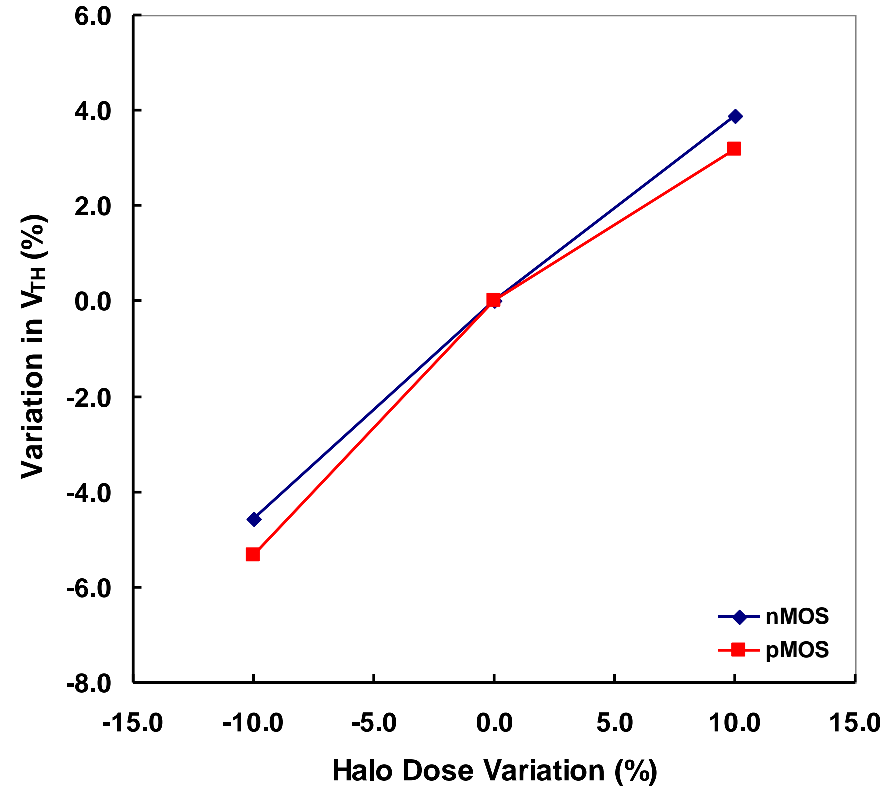
© 2008 Synopsys, Inc.

SYNOPSYS® Predictable Success

45 nm process variation

Gate Length and Halo dose Variation



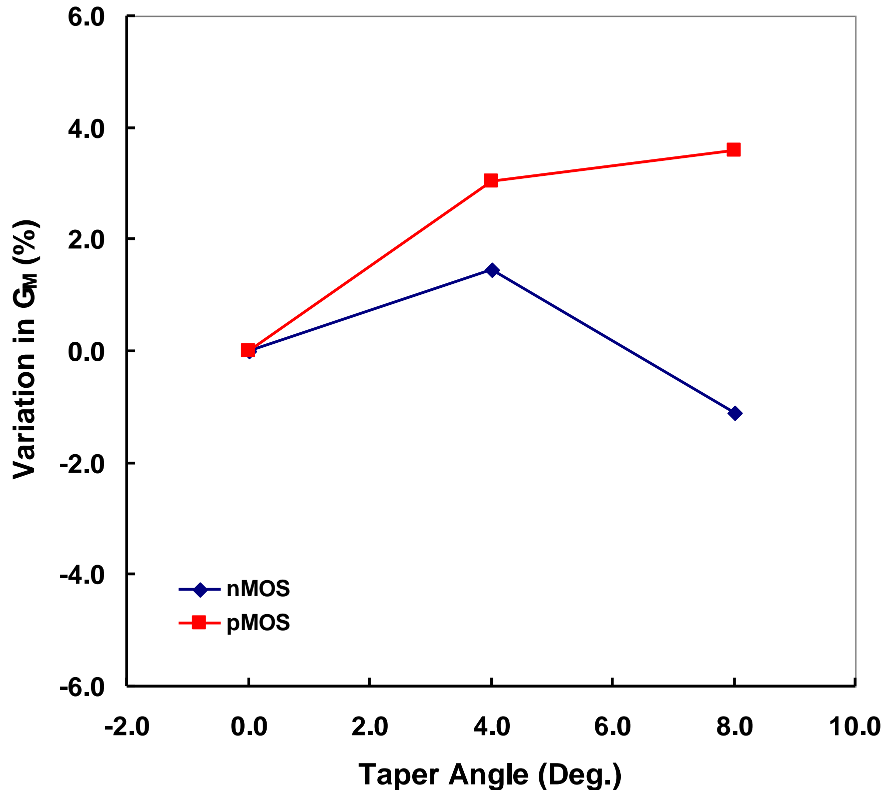


Transconductance Variation **Threshold Voltage Variation**

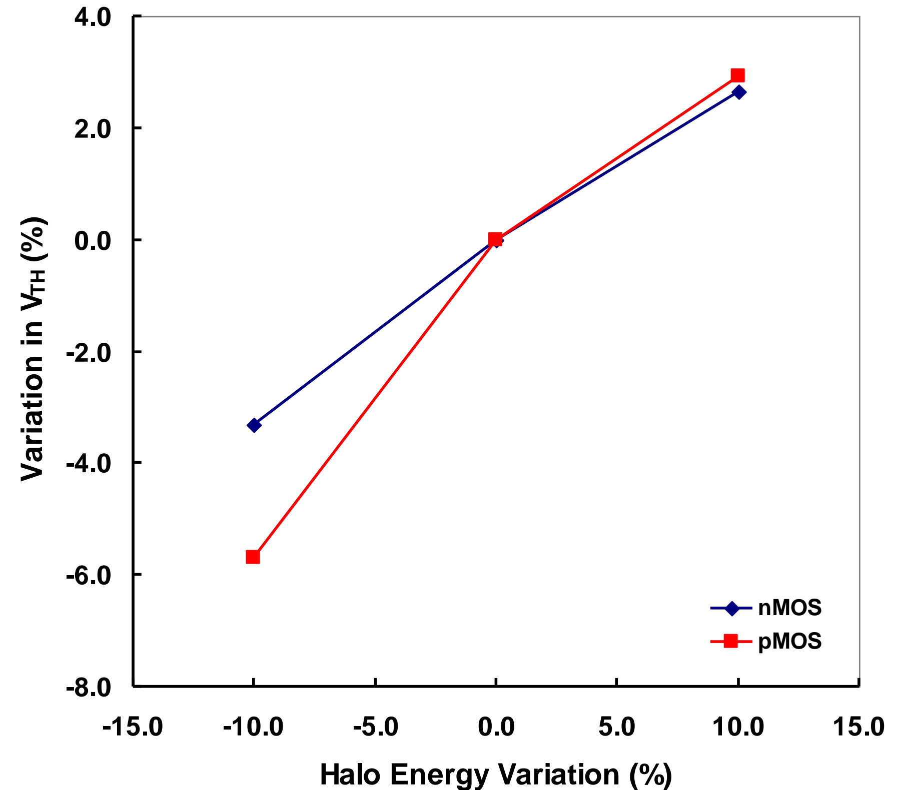
© 2008 Synopsys, Inc. (17)

45 nm process variation

Taper Angle and Halo Energy Variation



Transconductance Variation



Threshold Voltage Variation

© 2008 Synopsys, Inc. (18)

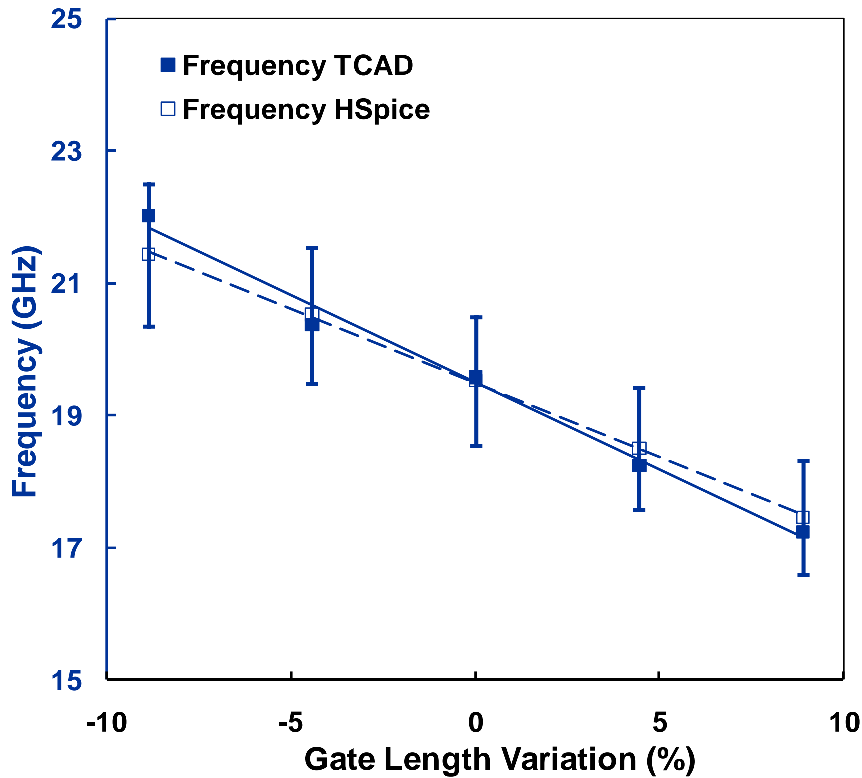
Outline

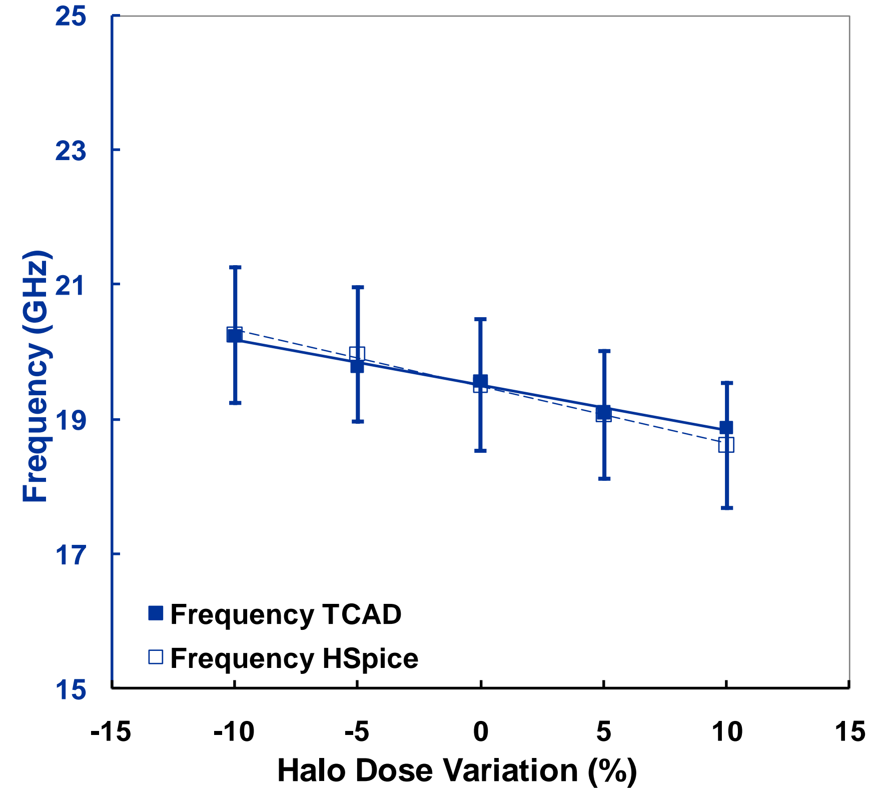
- Process variability and impact of process variability
- Process aware-spice models
- The 45 nm process flow
- Process aware parameter extraction for the 45 nm process
- **Circuit simulation results**
- Summary and conclusions

SYNOPSYS®
Predictable Success

5 Stage Ring Oscillator

Frequency



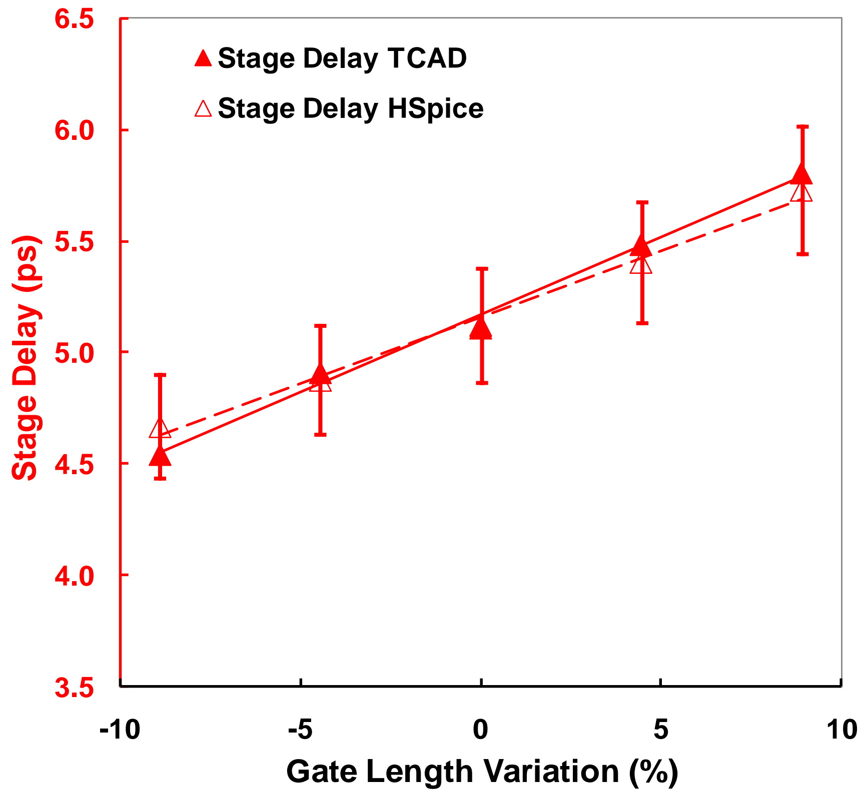


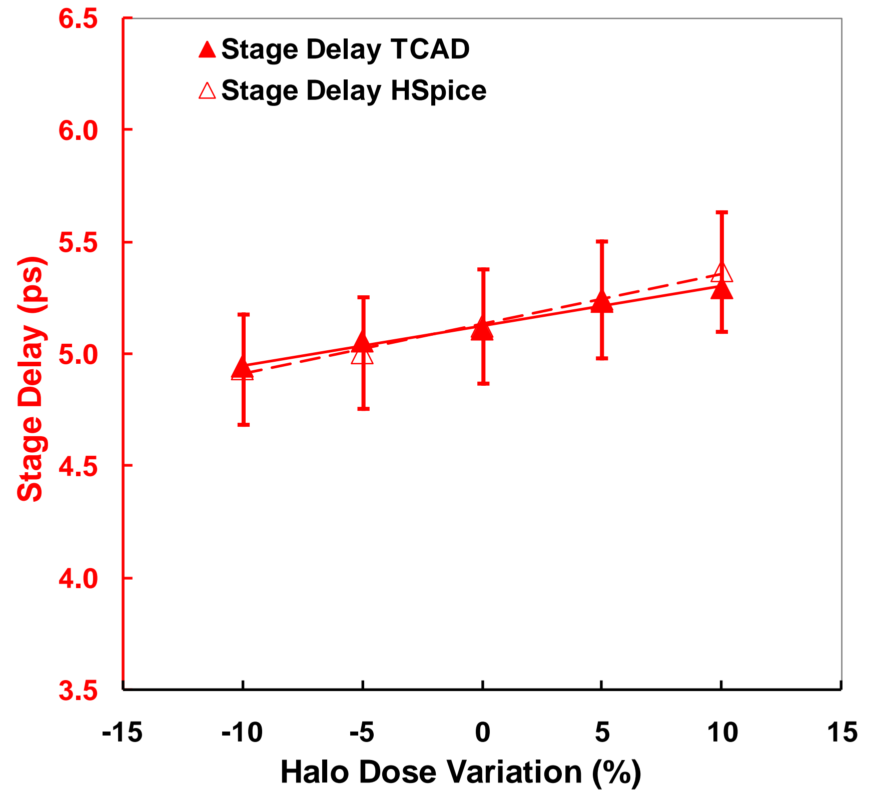
Gate Length Variation **Halo Dose Variation**

© 2008 Synopsys, Inc. (20)

5 Stage Ring Oscillator

Stage Delay





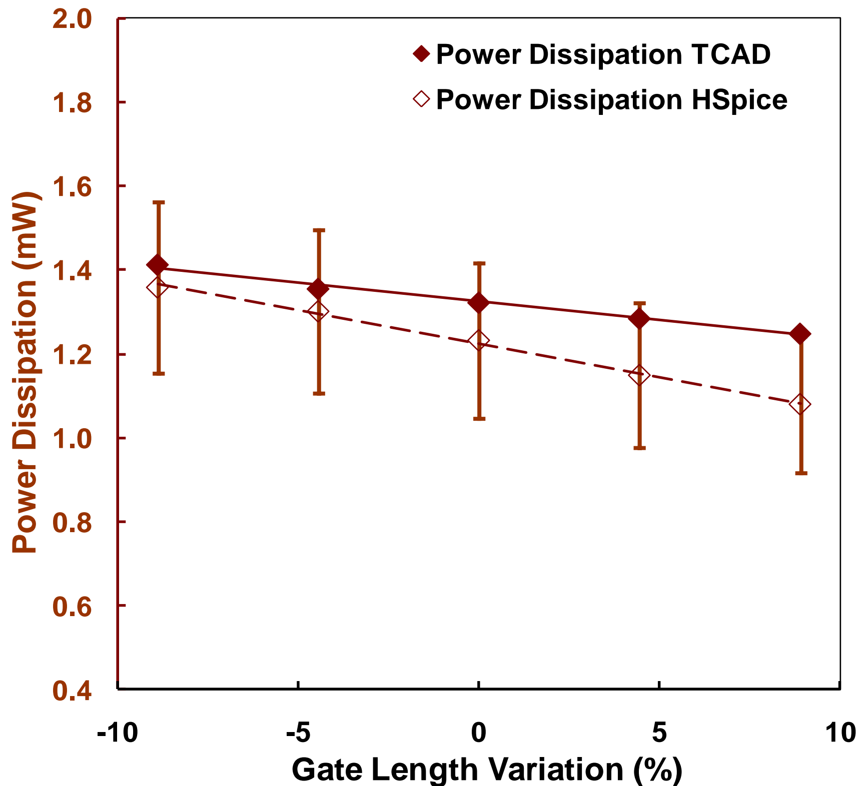
Gate Length Variation

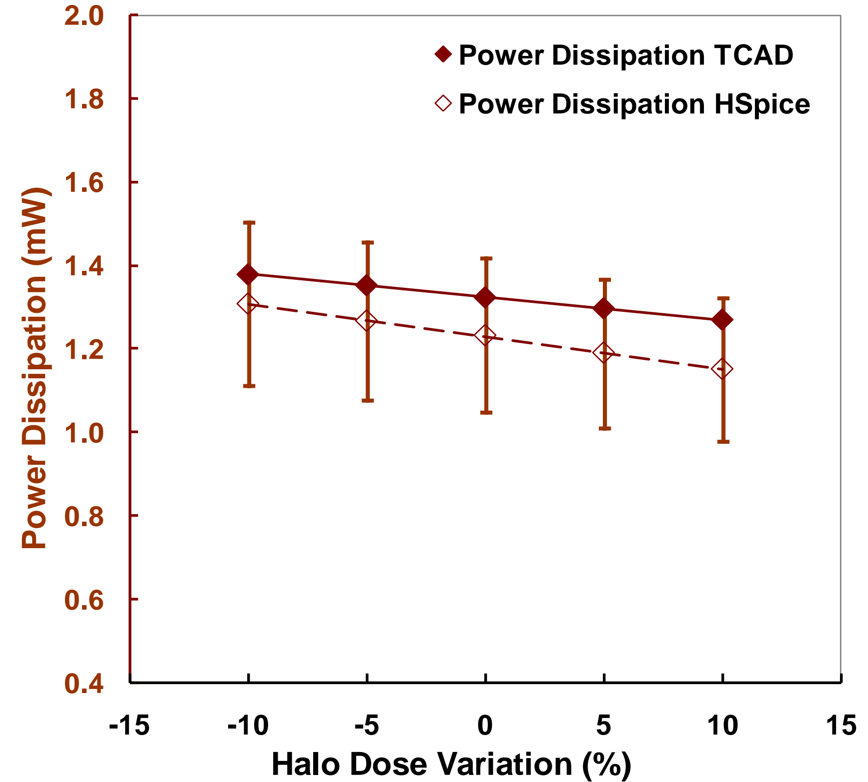
Halo Dose Variation

© 2008 Synopsys, Inc. (21)

5 Stage Ring Oscillator

Power Dissipation





Gate Length Variation

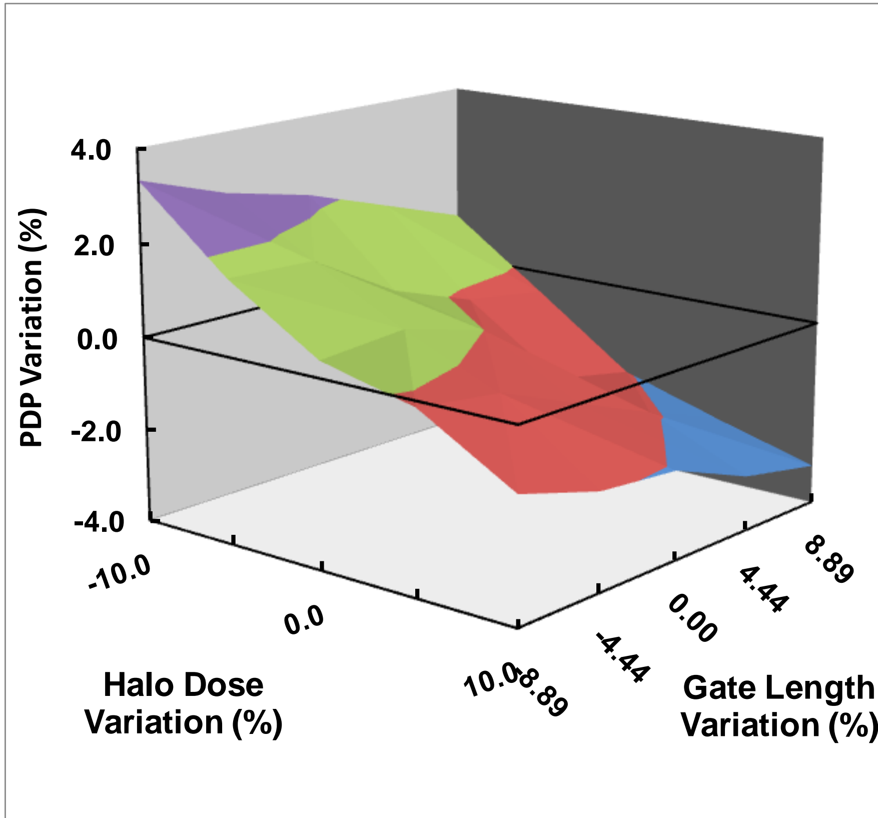
Halo Dose Variation

© 2008 Synopsys, Inc. (22)

SYNOPSYS®
Predictable Success

Prediction with the model

Delay – Power Dissipation product variation with process



- The variation of the Delay – Power Dissipation product as a function of gate length variation and halo dose variation is shown
- This plot can be used to optimize the design in terms of power dissipation and delay and identify the sweet spot

© 2008 Synopsys, Inc. (23)

SYNOPSYS® Predictable Success

Outline

- Process variability and impact of process variability
- Process aware-spice models
- The 45 nm process flow
- Process aware parameter extraction for the 45 nm process
- Circuit simulation results
- **Summary and conclusions**

SYNOPSYS®
Predictable Success

Summary and conclusions

Process Aware SPICE models

- **Enables engineers to consistently optimize process and design.**
- **Minimizes split lot experiments to identify a sweet spot for a given design.**
- **Provides more controls over the existing power and performance related constraints, to help optimize for a robust design**

Minimal experimental efforts

- **Results in significant productivity improvements**

© 2008 Synopsys, Inc.

SYNOPSYS®
Predictable Success

SYNOPSYS®

Predictable Success

SYNOPSYS®
Predictable Success