MOSFET Compact Modeling Issues for Low Temperature (77 K - 200 K) Operation

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Outline

- Introduction
- CMOS process and characterization
- Results concerning standard and specific effects at low temperature
- Compact modeling issues at low temperature
- Conclusion

Introduction: aim of this work

- ✓ **Design of hybrid CMOS read-out circuits for night vision with high perf. IR detectors**
- ✓ **Difficulties: low temperature (LT) & analog (weak/moderate inversion) circuits**
- ✓ **EKV2.6 used for IC design with 0.8 … 0.35 µm CMOS**
- ✓ **More and more transistors in the pixel, need for advanced CMOS processes**
- ✓ **0.18 µm process: new effects, e.g. INWE (STI), DITS (pockets)**
- ✓ **Need an accurate compact model, which model: EKV3 (charge), HiSIM2 or PSP (surface potential)?**

CMOS process & characterization

Process

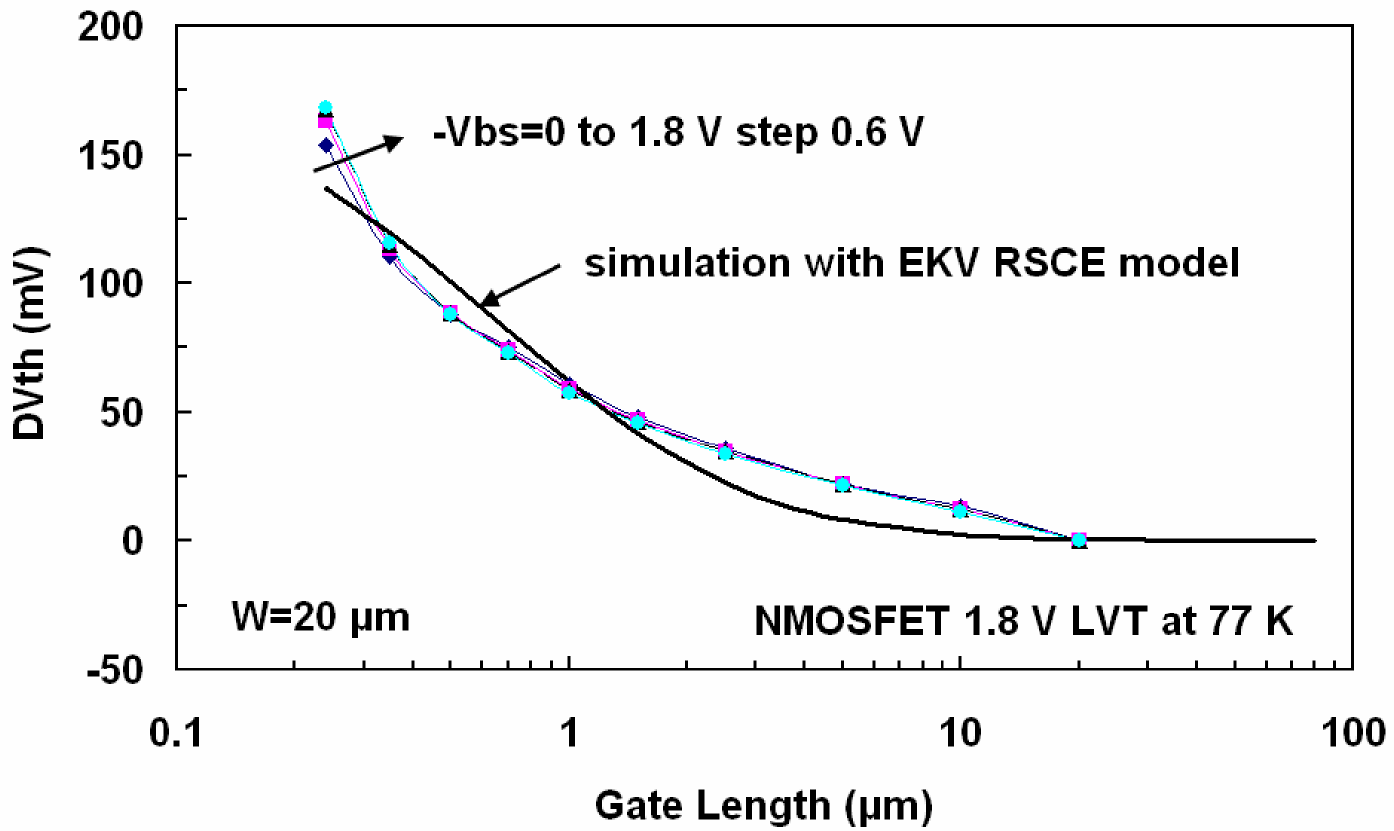
- ✓ Commercial process, optimized for room temperature
- ✓ 0.18 µm - 1.8 V (Tox=3.3 nm) & 0.35 µm - 3.3 V (6.5 nm)
- ✓ Different transistors: standard (STD), low Vth (LVT), zero Vth (ZVT)

Characterization

- ✓ 1st step before parameter extraction & optim. using a compact model
- ✓ Short channel effects
- ✓ Narrow width effects
- ✓ Evolution of std. effects, temperature range: 77 K – 300 K
- ✓ Specific effects at LT ?

Reverse short-channel effect (RSCE)

DVth = Vth - Vth (L=20 µm)

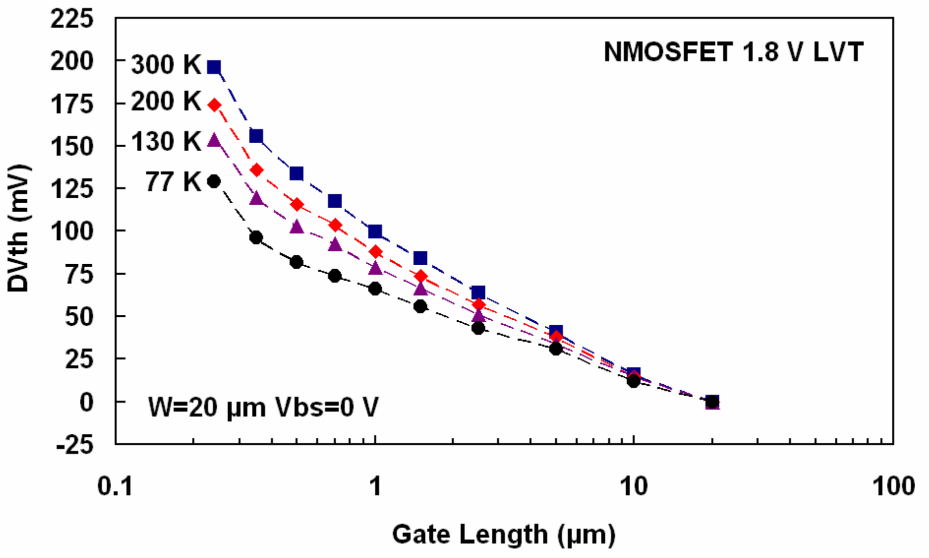


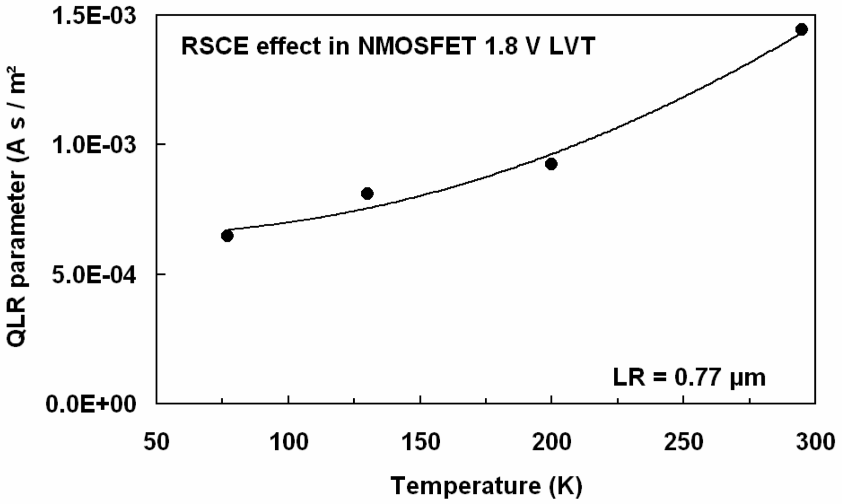
Standard RSCE effect well modeled in EKV2.6 and EKV3

Temperature modeling of RSCE effect

- **RSCE reduced by temperature lowering**
- **Interpretation: Vth function of 2 Φ_F**

$$\Phi_F(L) = \frac{kT}{q} \mathrm{Ln}\left(\frac{N_{ch}^{eff}(L)}{n_i}\right)$$

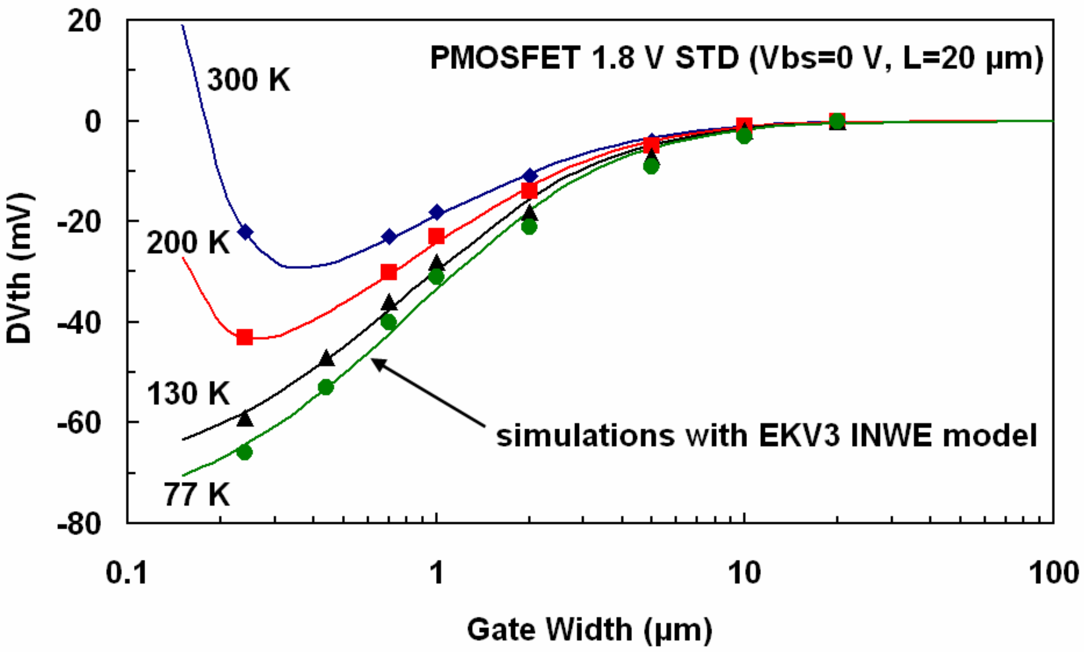


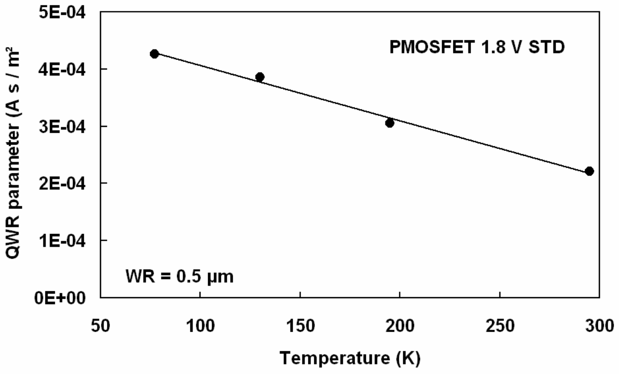


Evolution of QLR with T: quadratic law

EKV2.6 and EKV3 model parameter

Inverse narrow width effect (INWE)

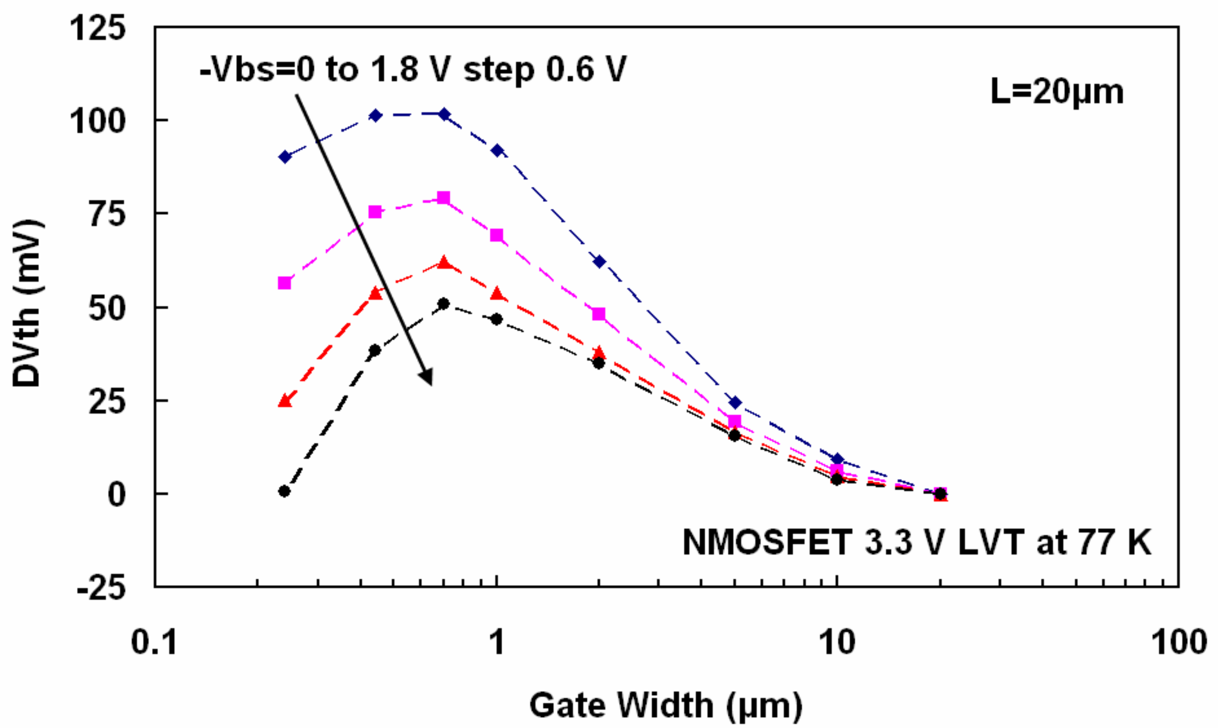




- **INWE due to STI**
- **Increased by temperature lowering**
- **Not modeled in EKV2.6, but modeled in EKV3**
- **Linear evolution with temperature of QWR, the EKV3 model parameter**

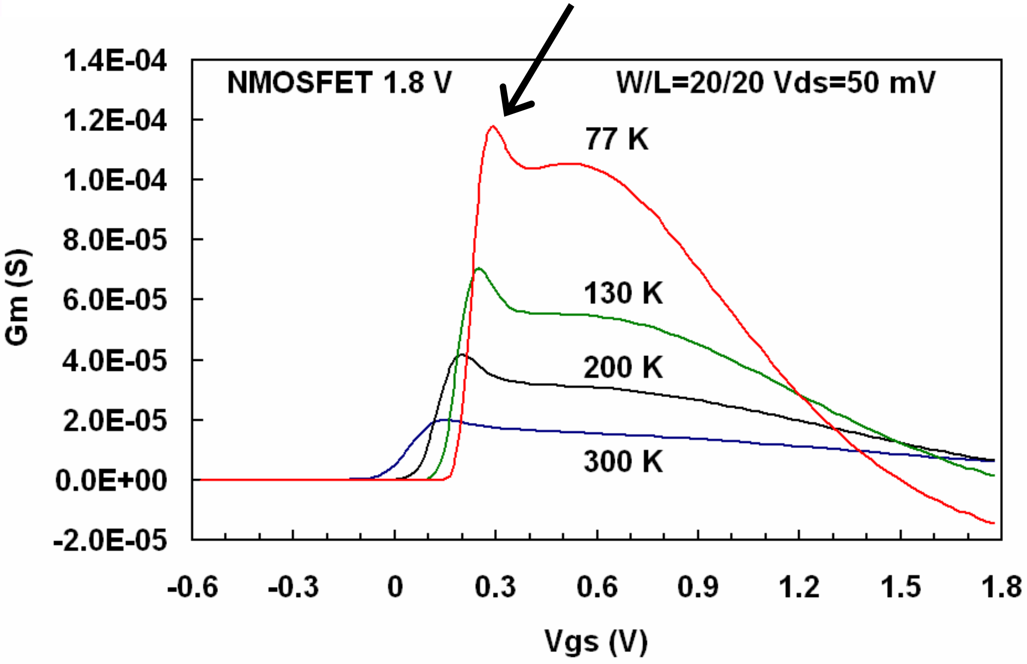
Specific effects at low temperature ?

Anomalous INWE



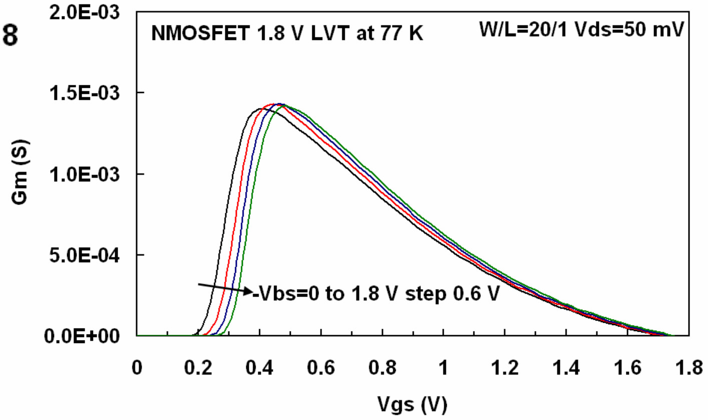
- Observed only in NMOSFETs, also at 300 K
- Max DVth: 20 mV at 300 K, 60 mV at 130 K (Vbs = 0 V)
- Origin ?
- Anomalous effect not modeled in EKV3, HiSIM or PSP

Observation of a Gm peak at LT



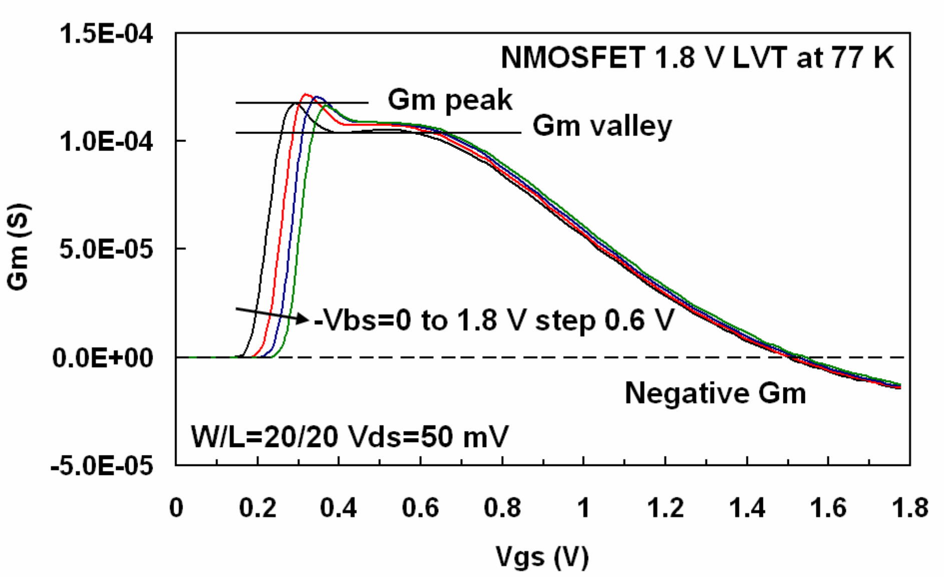
L=20 µm

L=1 µm



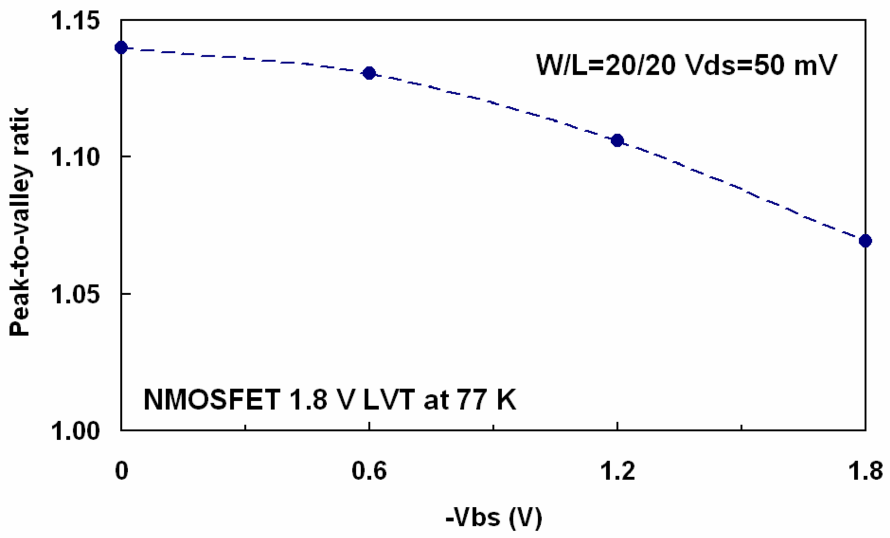
Peak observed in moderate inversion, only on LVT NMOS transistors (lowly doped), only on long channels, not on short channels

Origin of the Gm peak ?



Measurements done at different Vbs

The peak-to-valley ratio tends to 1 at high Vbs



Tentative interpretation of the Gm peak

- **2D-quantization in the inversion layer due to surface field Fs**
- **Formation of energy subbands**

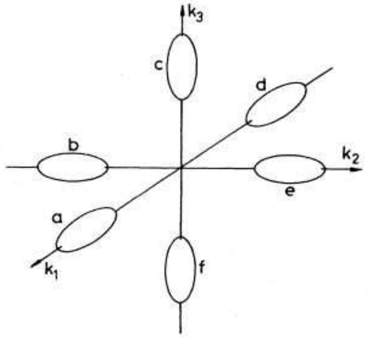


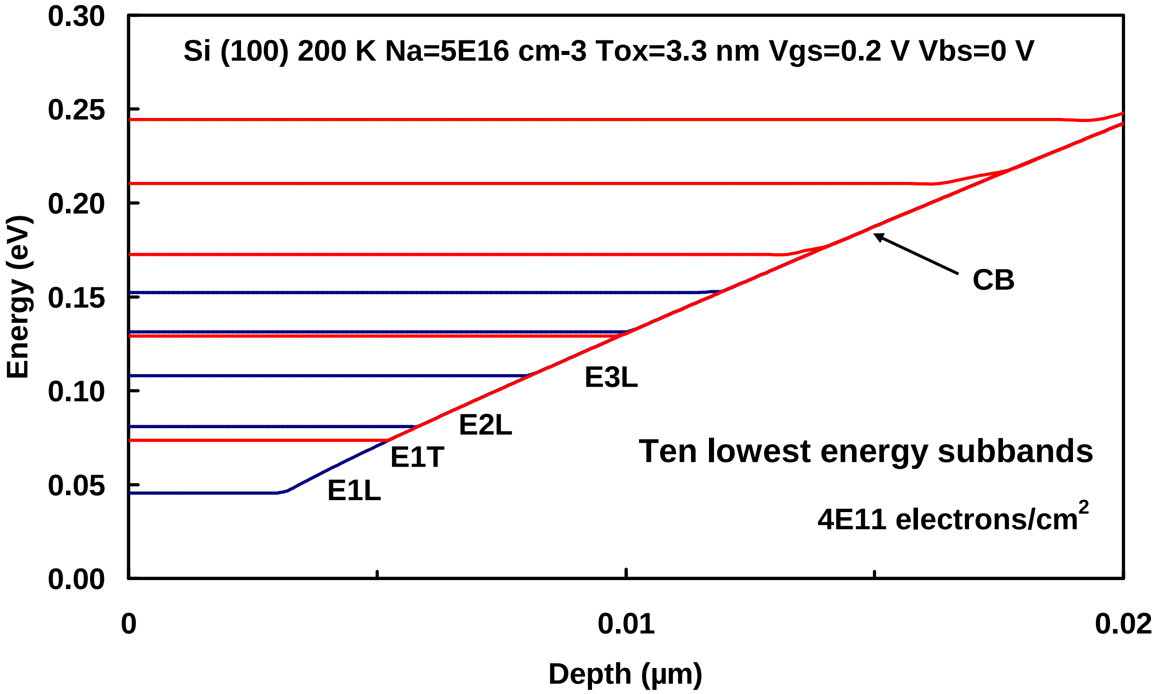
FIG. 5. Schematic constant-energy surfaces for the conduction band of silicon, showing six conduction-band valleys in the ⟨100⟩ direction of momentum space. The band minima, corresponding to the centers of the ellipsoids, are 85% of the way to the Brillouin-zone boundaries. The long axis of an ellipsoid corresponds to the longitudinal effective mass of electrons in silicon, $m_l=0.916m_0$, while the short axes correspond to the transverse effective mass, $m_t=0.190m_0$.

(Ando, 1982)

$m_T = 0.19\ m_0$

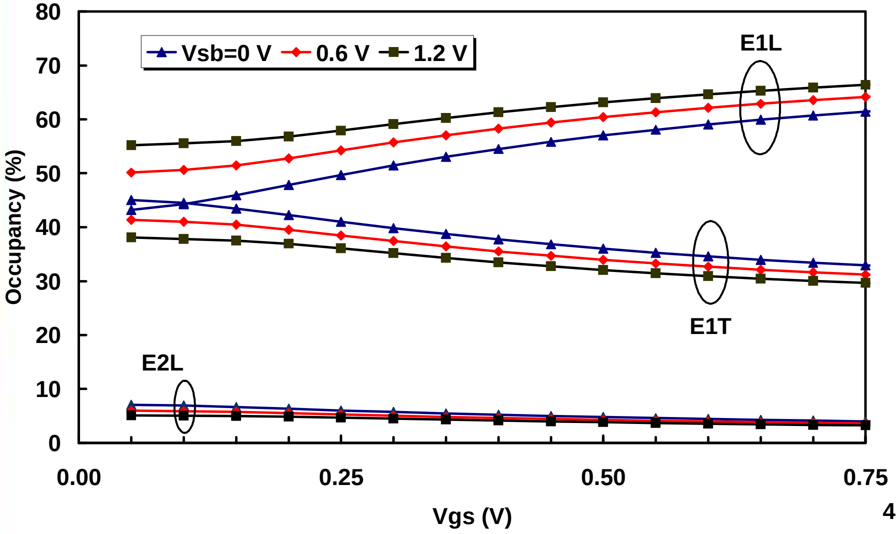
$m_L = 0.916\ m_0$

Poisson-Schrödinger simulations



Poisson-Schrödinger simulations

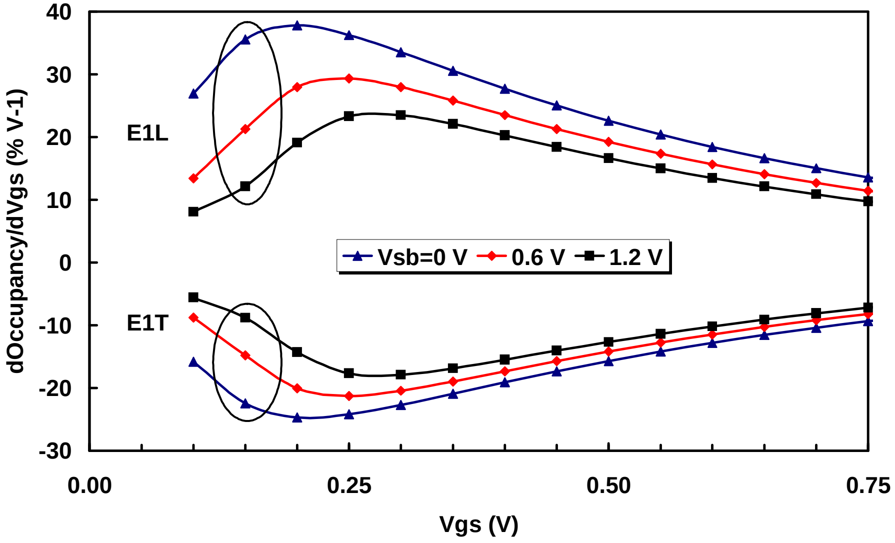
Influence of substrate biasing



Vsb↗ Qb↗ Fs↗ %E1L ↗

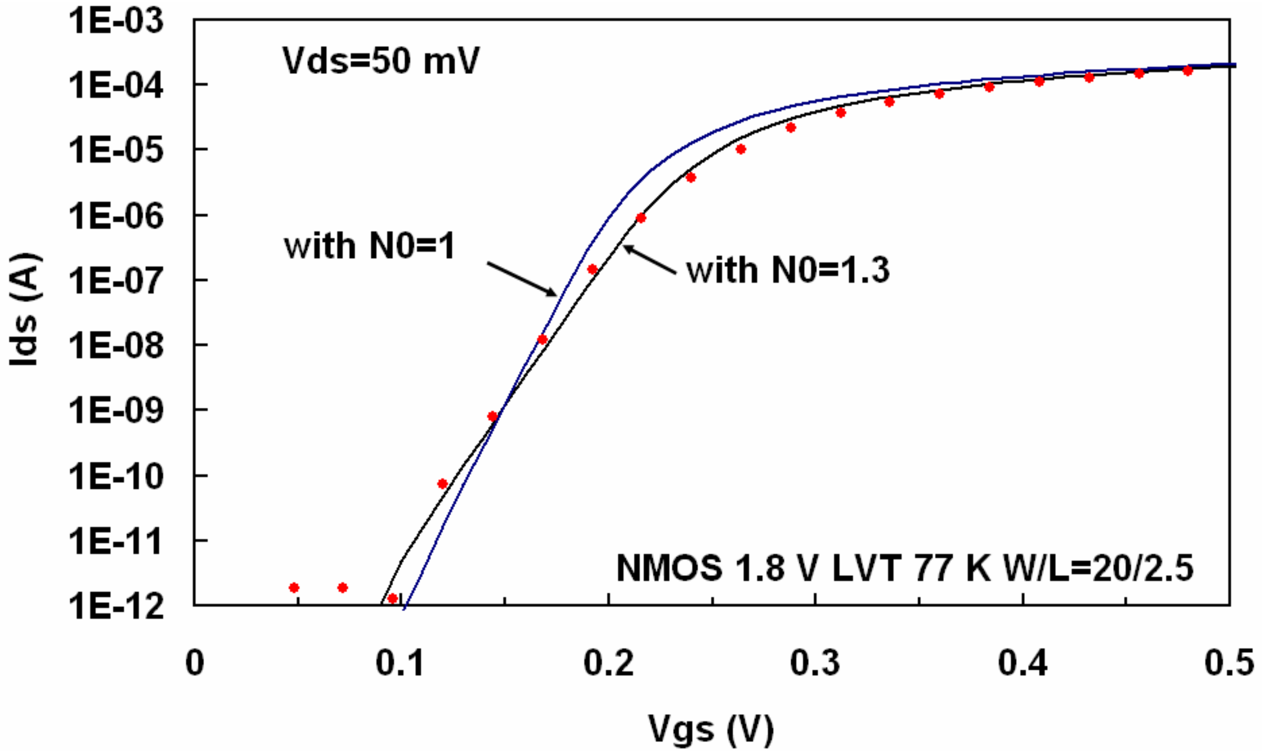
Ids ≈ Ninv

Gm ≈ dNinv/dVgs



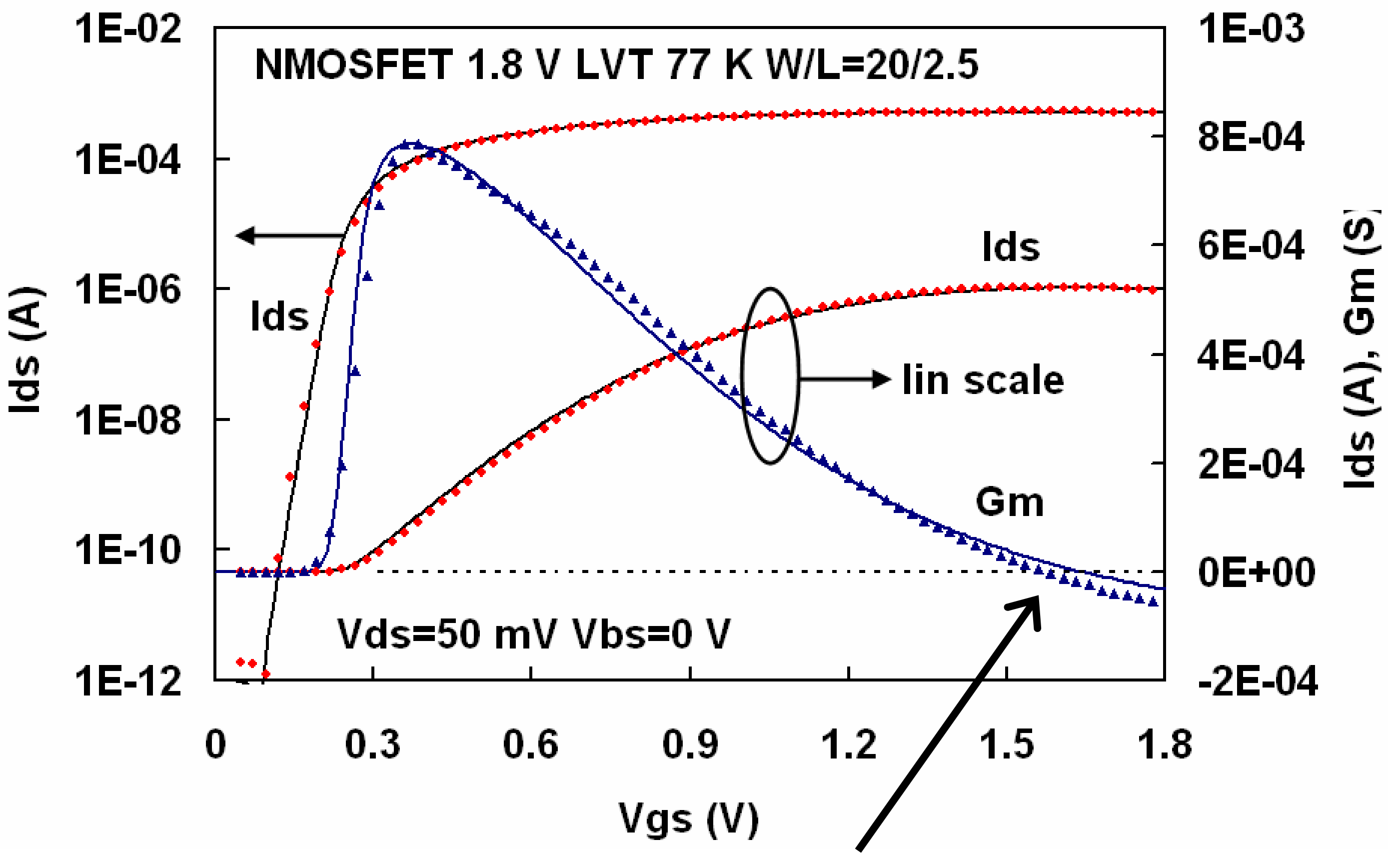
T=200 K Na=5x10^{16} cm^{-3}
Tox=3.3 nm

Subthreshold slope degradation at LT



- **S ≈ 20-25 mV/dec. at 77 K for long channels: higher than that predicted**
- **Influence of interface traps**
- **Need for a new parameter: N0 in EKV3, CT in PSP, PTHROU in HiSIM2**

Negative Gm and EKV3 simulation



- **Negative Gm on some transistors at LT**
- **Mobility model (incl. Coulomb scatt., phonons & SR) accounts for negative Gm observed on some transistors**

Others effects & modeling issues

- **Freeze-out in LDD zones: strong impact during parameter extraction at low Vds, not modeled in EKV, HiSIM or PSP**
- **DITS and Gds degradation in long channels (pockets): important for analog devices, but data only for room temperature**
- **Temperature modeling of GIDL (linear, STBGIDL parameter in PSP)**

Conclusion

- **Specific effects observed at low temperature, e.g.:**
  - ✓ **Quantization in inversion layer ⇔ Gm peak in some transistors**
  - ✓ **Freeze-out effects in LDD**
  - ✓ **Subthreshold slope degradation**
  - ✓ **Anomalous INWE**
- **Must be taken into account for accurate parameter extraction & modeling**
- **An improved compact model already needed for 0.18 µm technology**
- **EKV3 is a good candidate, but should be improved for accurate low temperature modeling and circuit simulations**
- **HiSIM2 and PSP to be evaluated at LT**