Compact layout and bias dependent base resistance model for advanced SiGe HBTs

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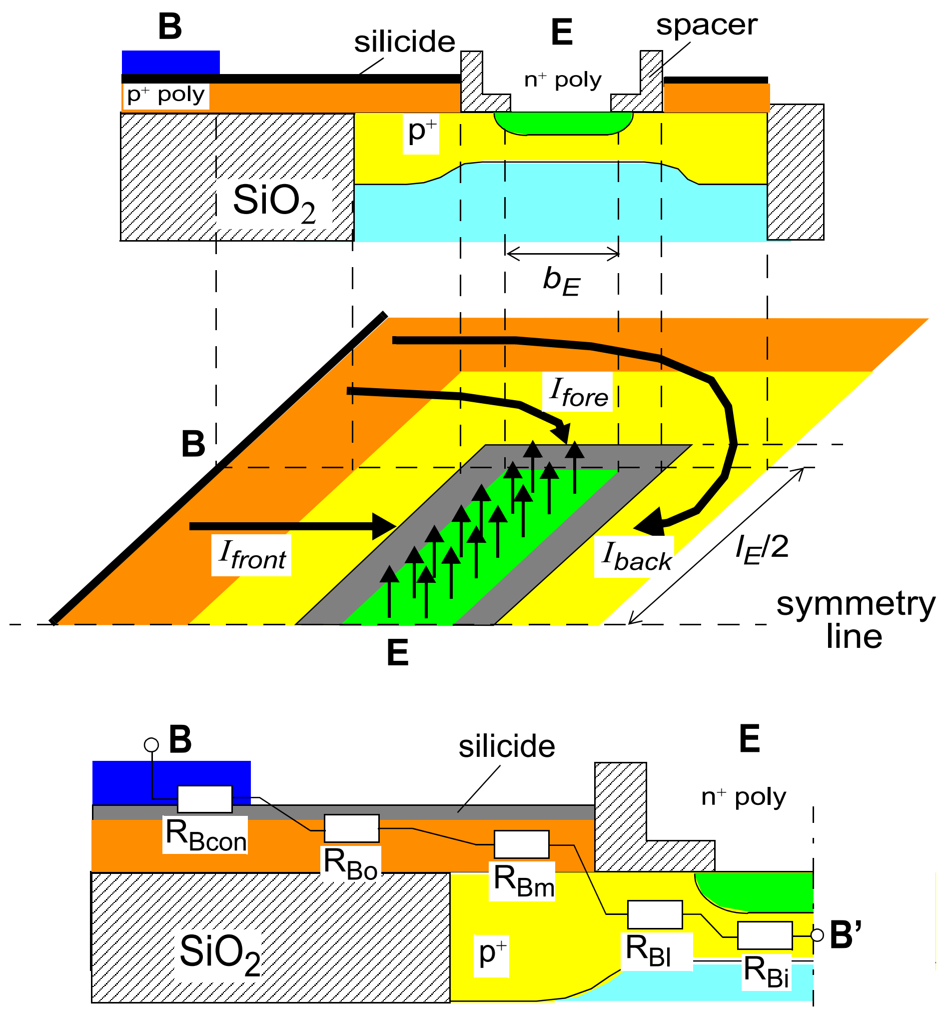
OUTLINE

- Introduction
- Method
- Investigated structures
- Simulations and model
- Results
- Conclusions

Base current flow and resistance components

- existing model from 1991/92 for BJTs with $r_{SI}/r_{SBi} \approx 0.2$
- advanced HBTs: $r_{SI}/r_{SBi} \approx 1$
  => deviations for $b_E/l_E > 1/5$ with existing model
- silicided external base region
  => single-base contact (SBC)
  => more widespread (space efficient)
- CMOS backend metallization
  => vias instead of slot contacts
- base contact perpendicular to emitter (e.g., SOI and implanted collector)
  => foreside-base contact (FBC)
  => not included in existing models



⇒ revisit existing equations and new development (FBC)

Method

- model current flow in 2D yz-plane
- sheet resistance in each region κ

$$r_{S\kappa} = (q\bar{\mu}_p \bar{N}_{B\kappa} L_x)^{-1}$$

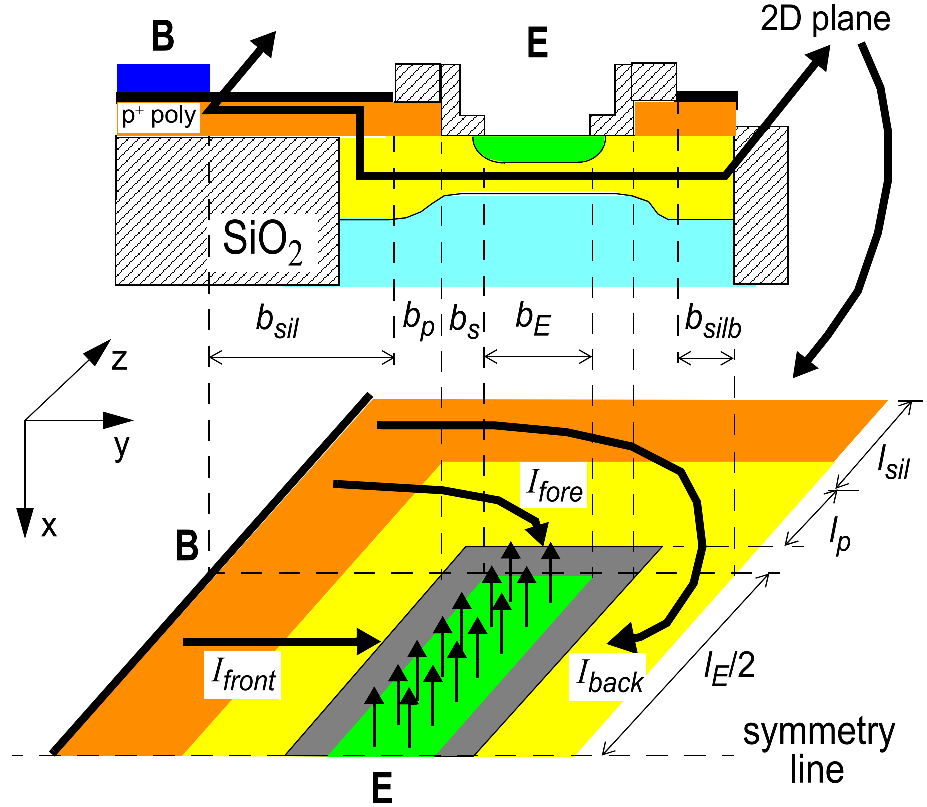
- voltage drop from transport eq.

$$r_S \vec{I}_p = -grad\varphi_p$$

$$\text{with} \quad \vec{I}_p = (I_{py}, I_{pz})$$

- continuity

$$div\vec{I}_p = -J_{SBi} \exp\left(\frac{\varphi_p}{V_T}\right)$$



⇒ **can use 2D device simulation**

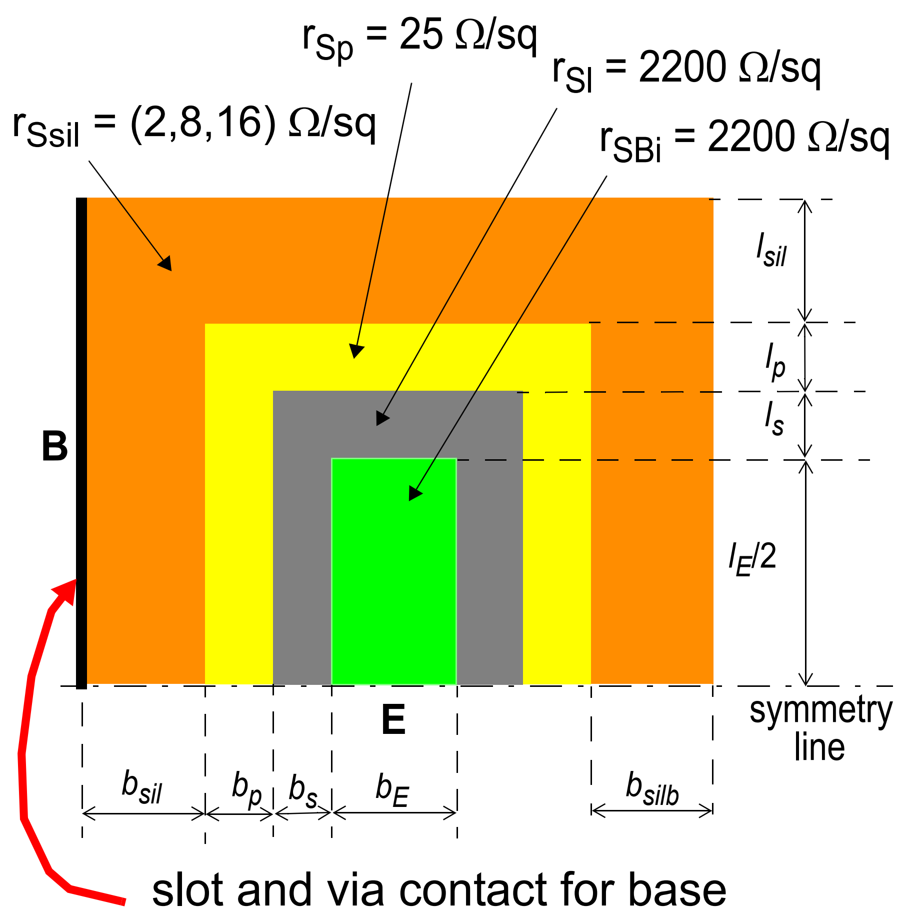
Investigated structures

- first set of structures (TED paper)
  - Double B contact parallel and perpendicular to emitter
  - single B contact parallel to emitter
  - ratio b_E/l_E = 0.02, 0.1, 0.17, 0.38, 1

	b_l	b_p	b_{sil}	l_p	l_{sil}	b_{silb}
value/μm	0.15	0.15	0.33 0.20	0.15	0.52 0.20	0.33 0.20
ratio to b_E	0.6	0.6	1.32 0.80	0.6	2.08 0.80	1.32 0.80

- second set of structures
  - single B contact parallel to emitter
  - foreside B contact: single and double
  - ratio b_E/l_E = 0.025, 0.05, 0.1, 0.2, 1.0

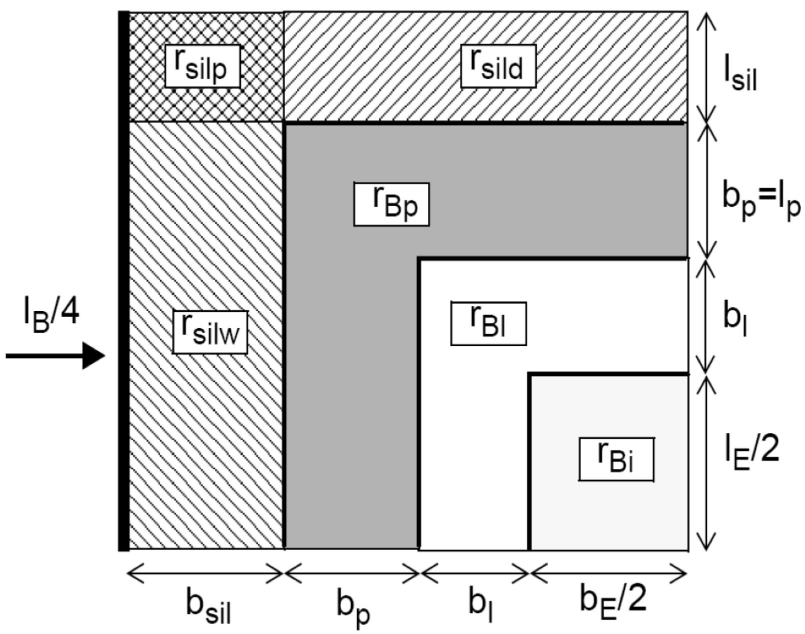
value/μm	b_l	$b_p = l_p$	b_{sil}	l_{sil}	b_{silb}	r_{Ssil}
case 1	0.15	0.15	0.2	0.2	0.2	8
case 2	0.15	0.15	0.1	0.1	0.1	8
case 3	0.15	0.15	0.1	0.1	0.1	16

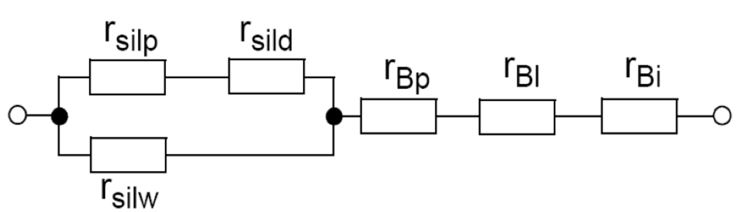


Simulations and model

Double-base contact (DBC) structures

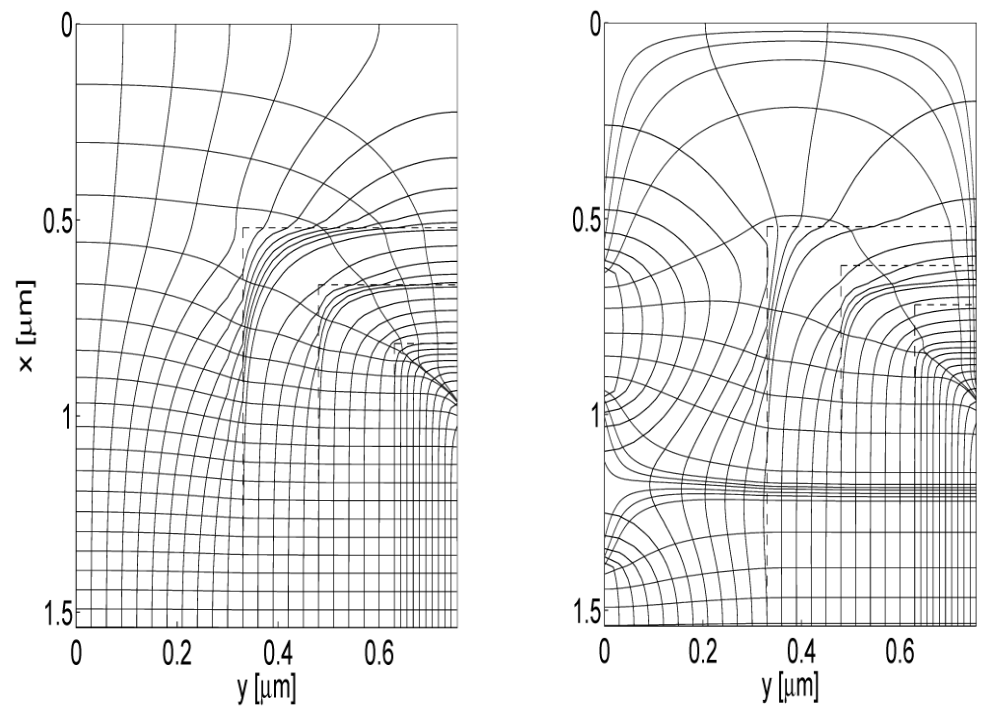
layout and equivalent circuit





flow and equipotential lines

slot contact $b_E/l_E = 0.38$ vias



⇒ current redistribution in silicide only

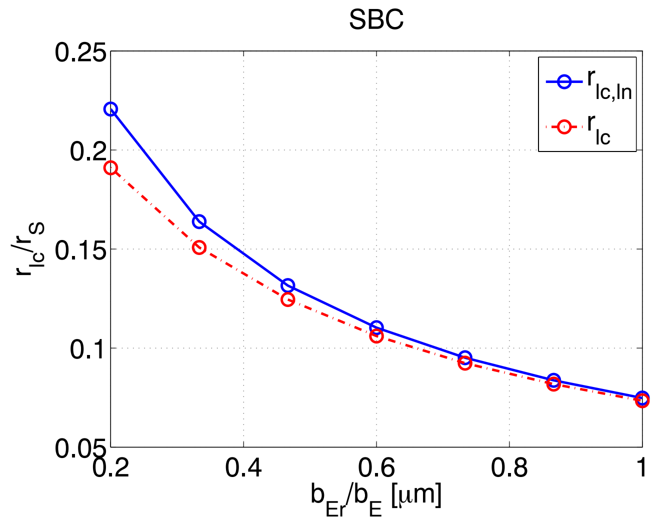
⇒ boundaries to link (spacer) and internal transistor are equipotential lines

Model: basic equations

- internal base resistance

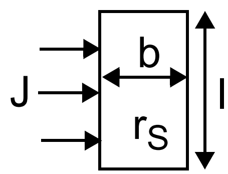
$$r_{Bi} = r_{SBi}\frac{b_E}{l_E}\, g_i(b_E, l_E)\frac{\ln(1+\eta)}{\eta}$$

includes conductivity modulation, layout dependence, emitter current crowding



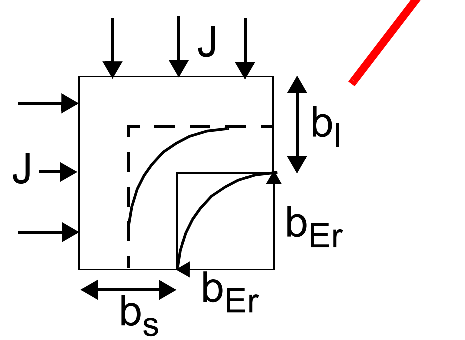
- parallel current flow perpendicular over boundary

$$r = r_S\frac{b}{l}$$



- corners (link resistance example)

$$r_{lc} = \frac{r_{Sl}}{2\pi}\ln\left(1+\frac{b_l}{b_{Er}}\right) \cong \frac{r_{Sl}}{2\pi}\frac{b_l}{(b_{Er}+b_l/2)}$$

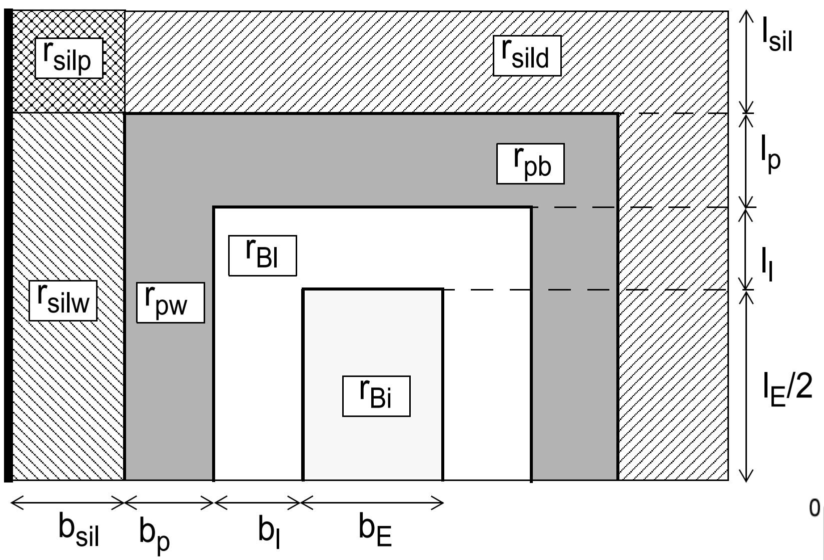


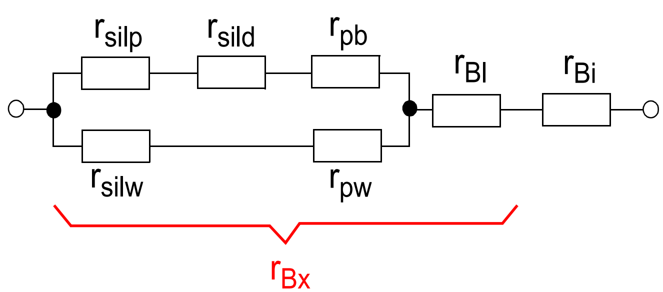
- distributed current flow => more details later

$\Rightarrow$ apply similarly to other regions and equivalent circuit elements

Simulations and equivalent circuit

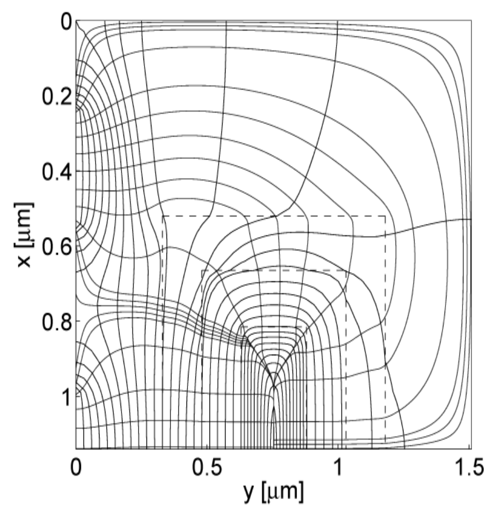
single base contact (SBC) structures

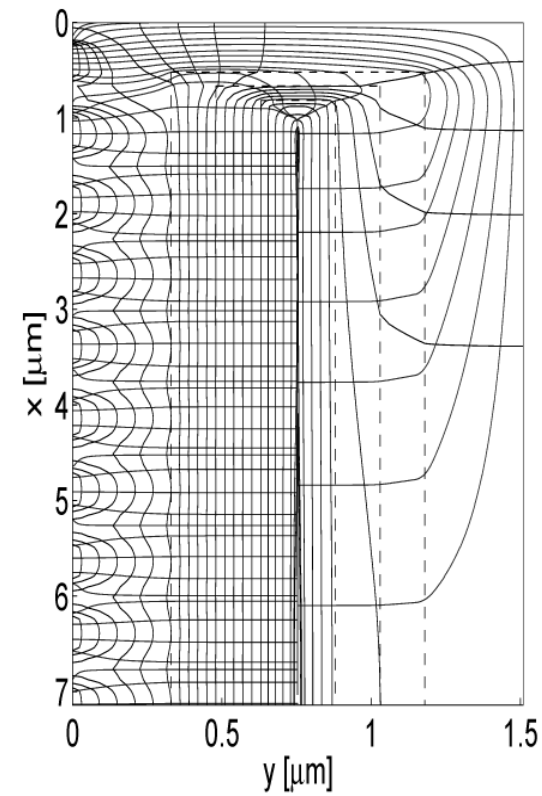




via contacts

$b_E/l_E = 0.38$





$b_E/l_E = 0.02$

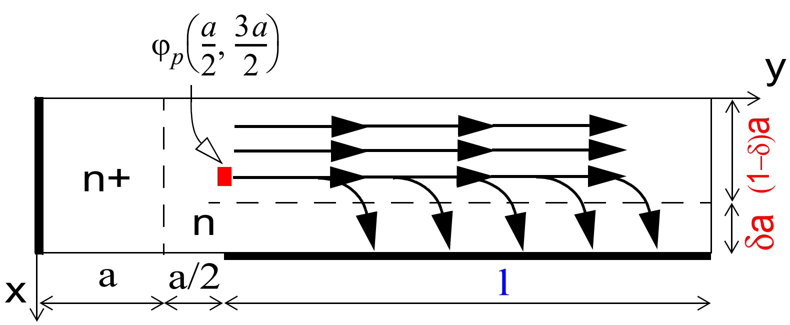
⇒ long structures suffer from silicide resistance (even at 2 Ω/sq)

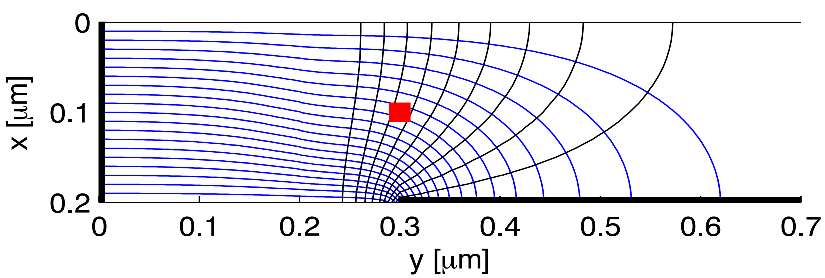
SBC structures / 2

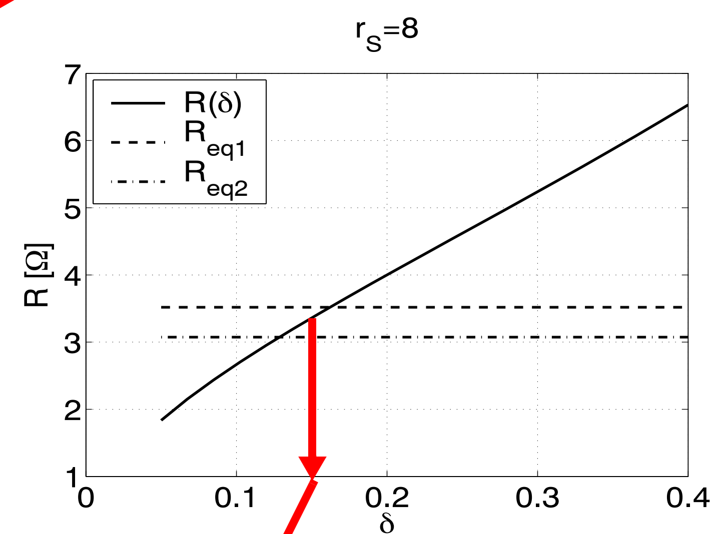
distributed current flow and associated resistance

$$r_{sild} = \frac{\varphi_p\left(\frac{a}{2}, \frac{3a}{2}\right)}{I} \overset{?}{=} \frac{r_{Ssil}}{2}\sqrt{\frac{\delta}{1-\delta}}\,\coth\left[\frac{l_E/2 + b_E + 3(b_l + b_p)}{l_{sil}\sqrt{\delta(1-\delta)}}\right]$$

1







⇒ partitioning factor is approximately 0.15

SBC structures / 3

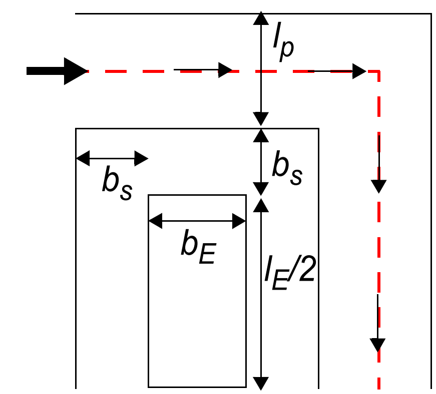
impact of distributed current flow on internal base resistance

- internal base resistance

  => change to one-sided value

$$g_i = \frac{1+3f_i}{12} - \left[\frac{1}{12} - \frac{1}{28.6}\right]\frac{b_E}{l_E}(1-f_i)$$

$$d_p = 3b_l + b_E + l_p + \frac{l_E}{2}$$



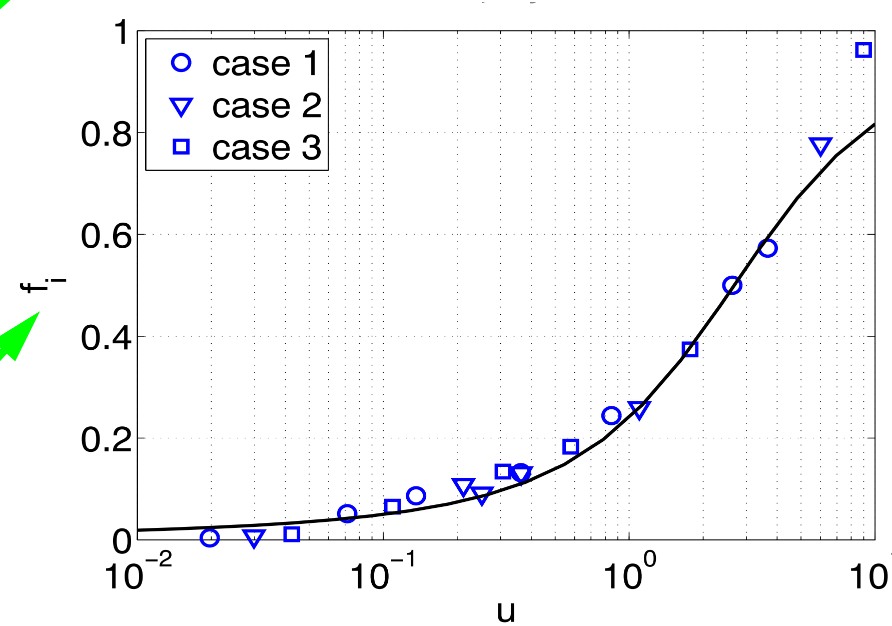
- transition variable (semi-empirical)

$$u = \ln\left(\frac{\left(\frac{b_{sil,b}}{r_{Ssil}(d_p + 2l_p + b_{sil,b})} + \frac{b_p}{r_{Sp}d_p}\right)^{-1}}{r_{SBi}(b_E/l_E)}\right)$$

- transition function

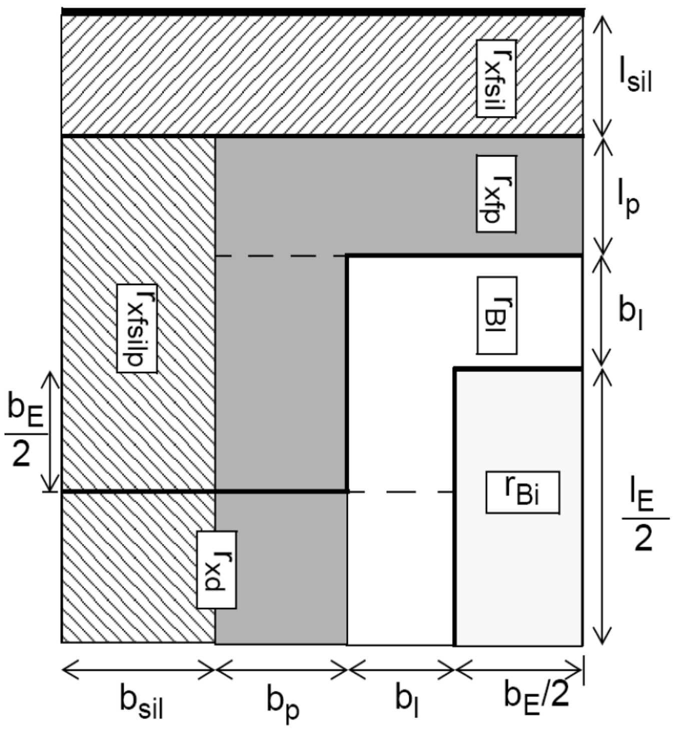
$$f_i(u) = a_{fi}[(u-u_0) + \sqrt{(u-u_0)^2 + e_{fi}}] - a_{fi}[(u-u_1) + \sqrt{(u-u_1)^2 + e_{fi}}]$$

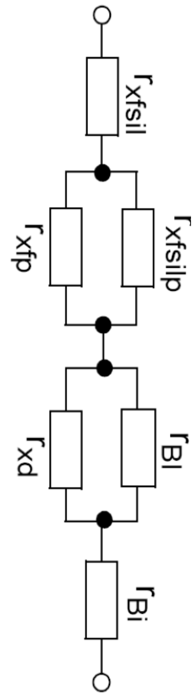
with a_{fi} = 0.65, u_0 = 0.6, e_{fi} = 2.5, $u_1 = u_0 + 1/(2a_{fi})$



Simulations: Foreside base contact (FBC) structures

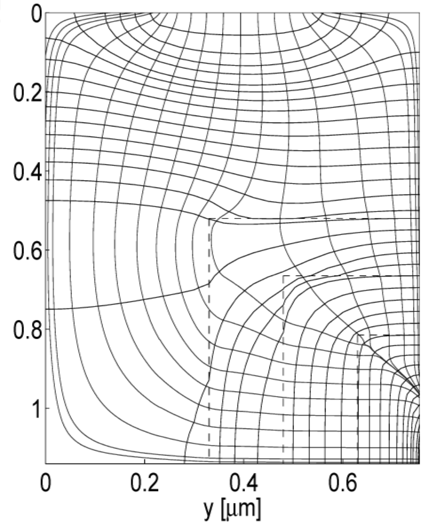
2 base contacts

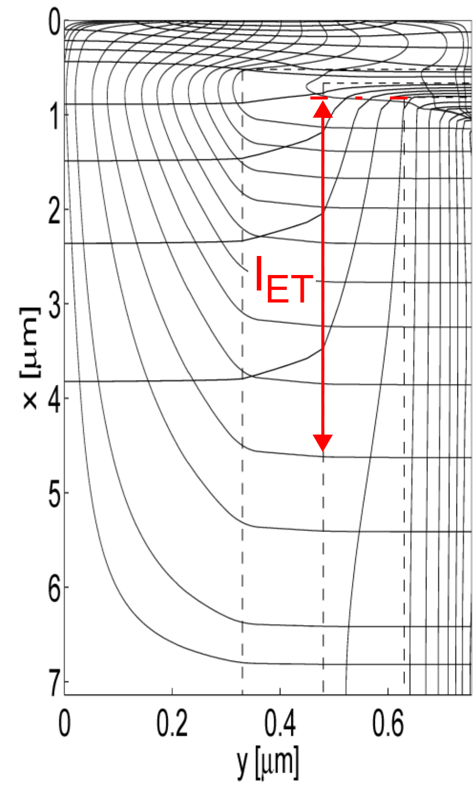




via contacts

$b_E/l_E = 0.38$





$b_E/l_E = 0.02$

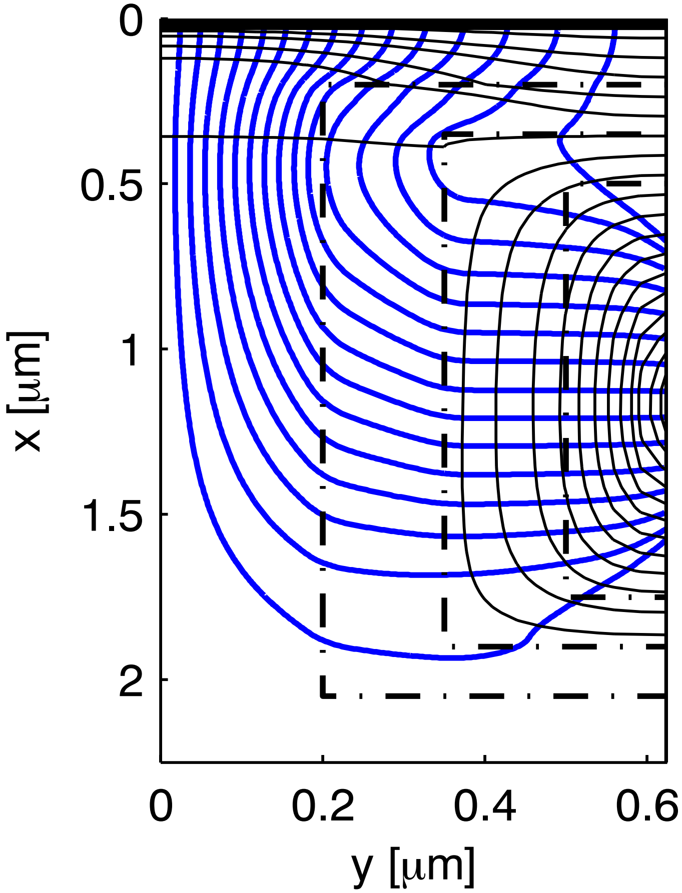
$\Rightarrow$ front side current fades beyond "transfer length"

Simulations: FBC structures

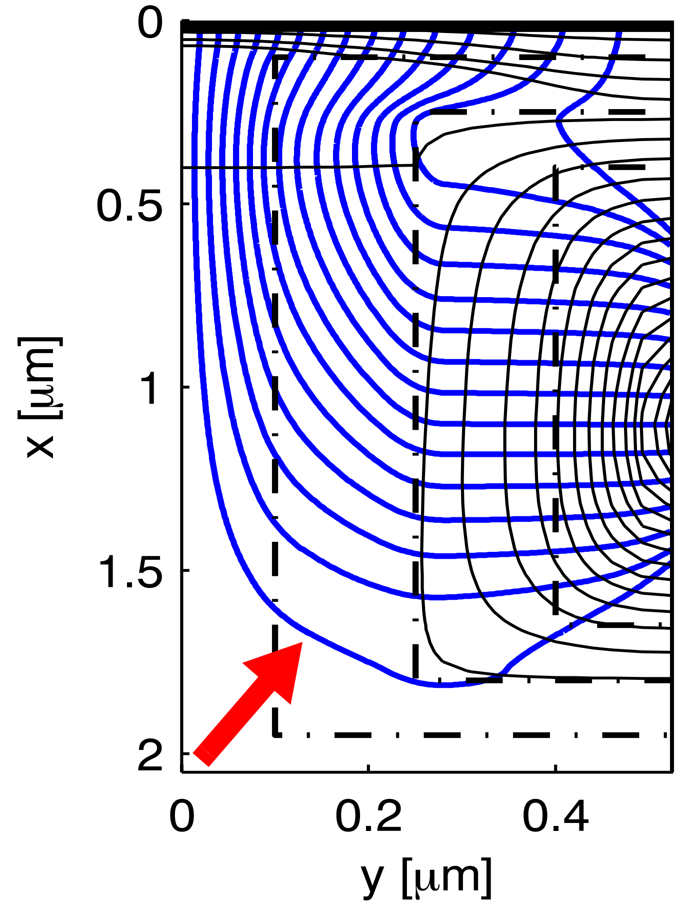
1 base contact (slot)

$b_E/l_E = 0.1$

wide silicide



narrow silicide

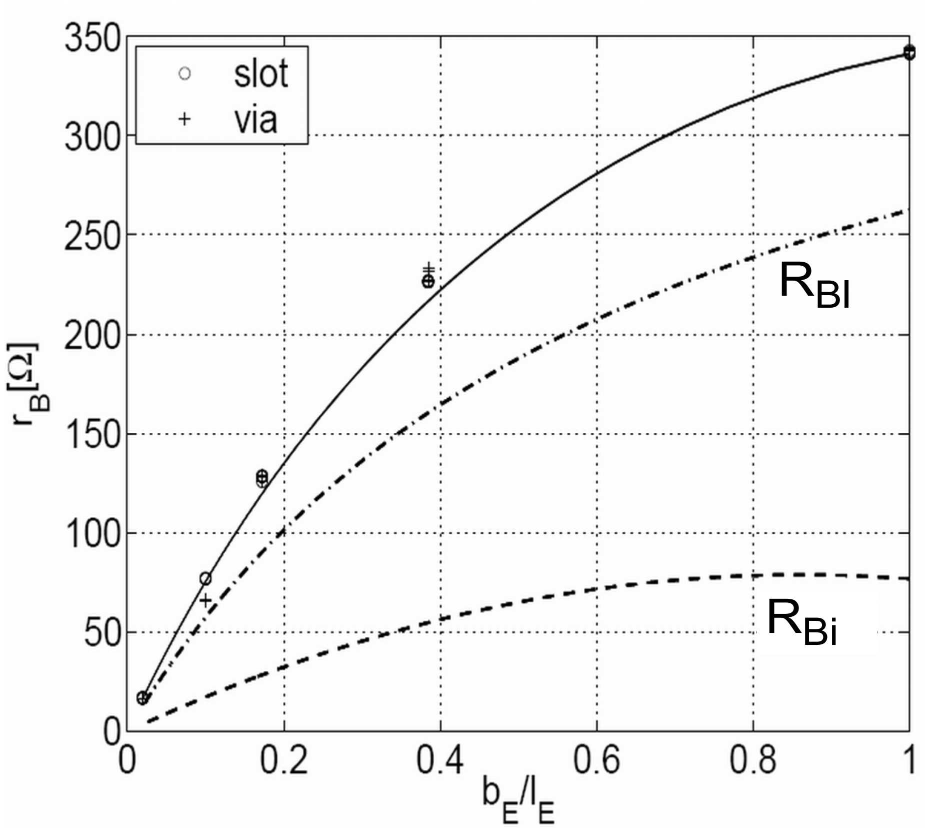


⇒ flow lines pushed into the poly layer => include in distributed resistance

Results

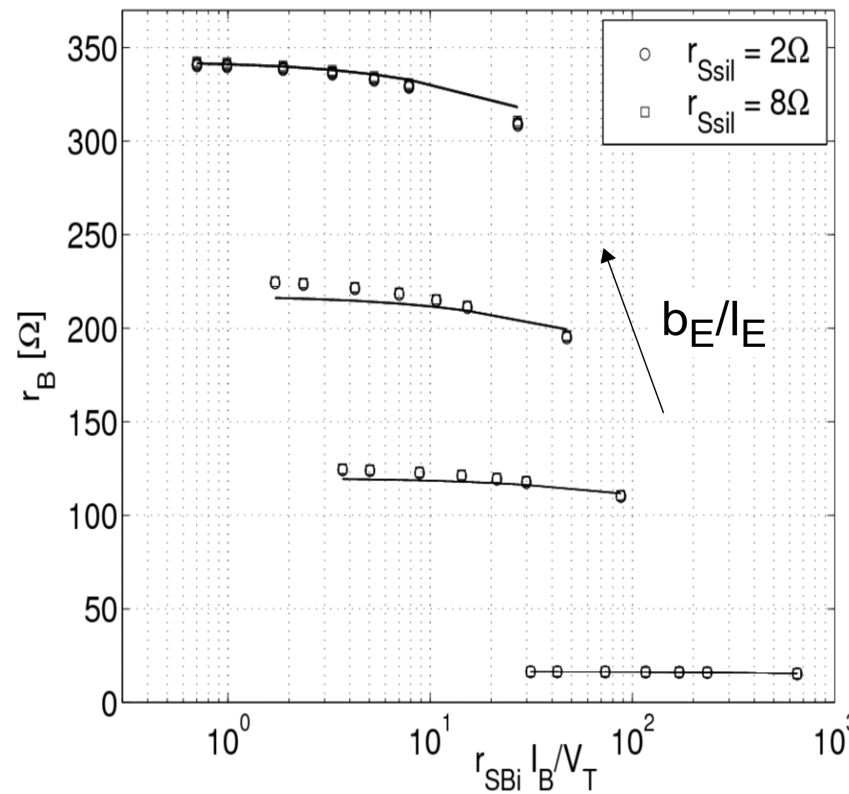
Total base resistance and components for DBC structures

... emitter aspect ratio



=> negligible impact of vias

... bias (normalized base current)



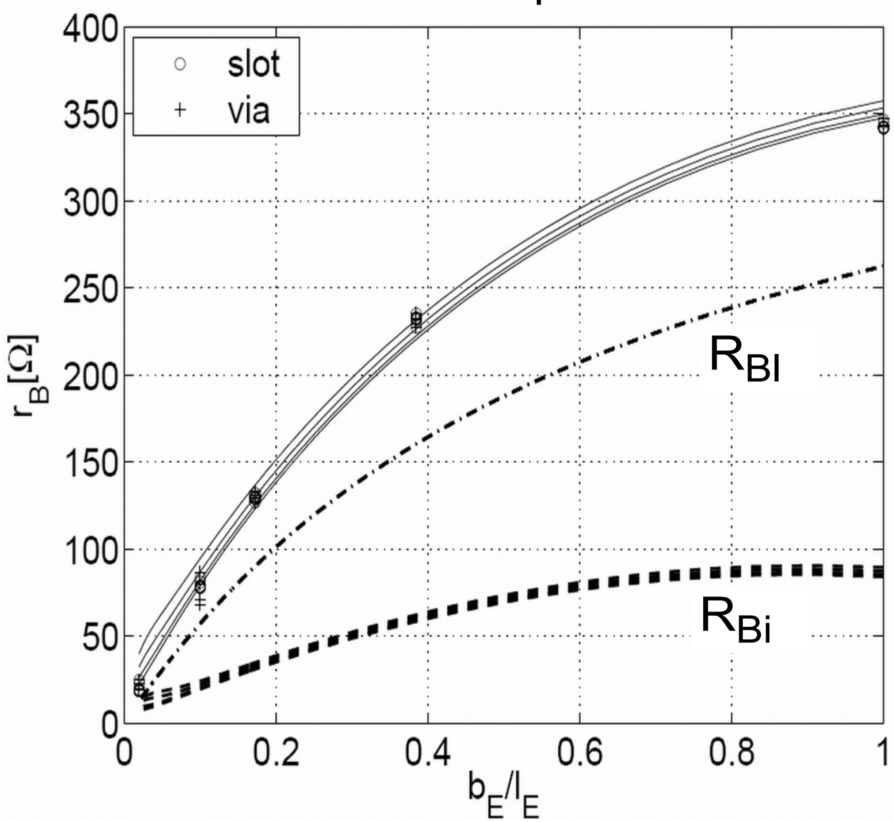
=> impact of emitter current crowding

⇒ good agreement over wide layout and bias range

Results / 2

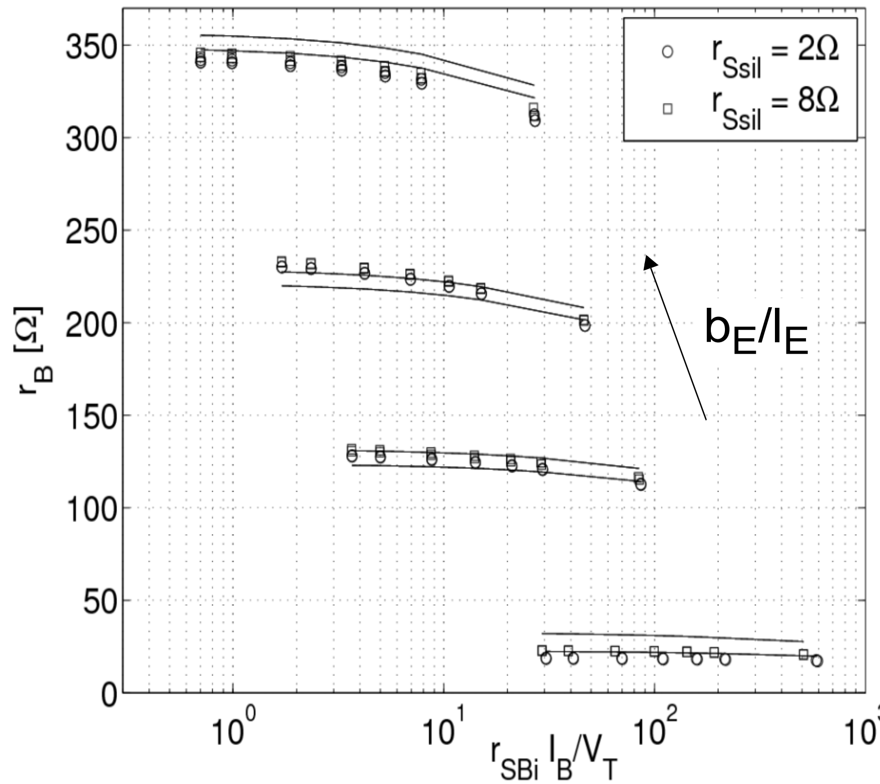
total base resistance of SBC structures versus ...

... emitter aspect ratio



=> negligible impact of vias

... bias (normalized base current)



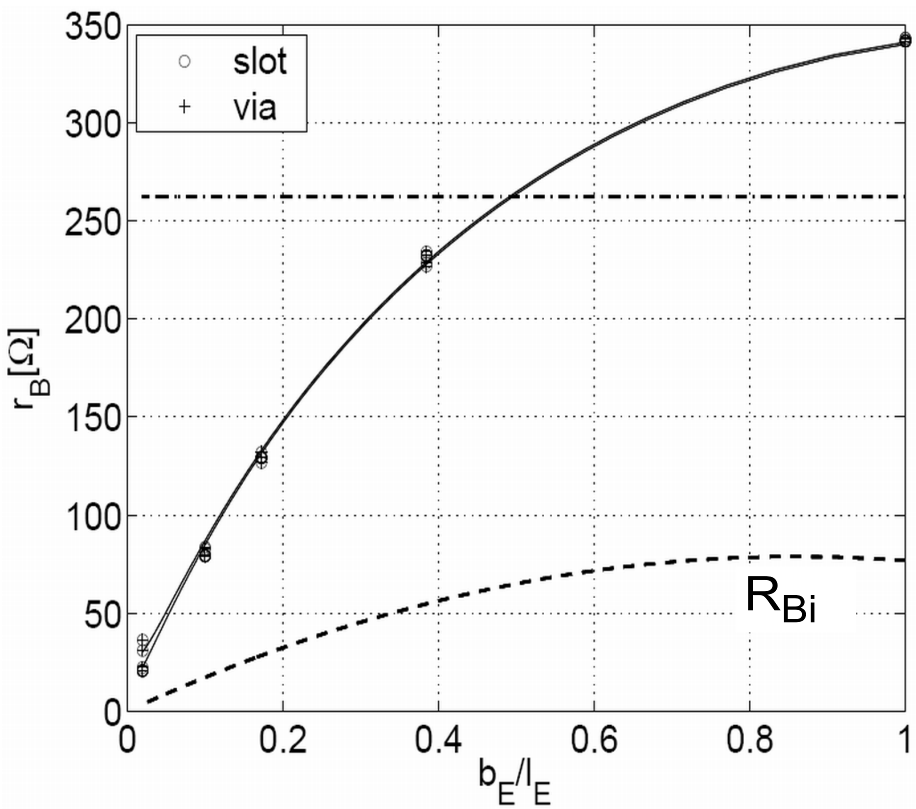
=> impact of emitter current crowding

⇒ good agreement over relevant layout, bias, sheet resistance range

Results / 3

total base resistance of FBC structures versus ...

... emitter aspect ratio



=> negligible impact of vias

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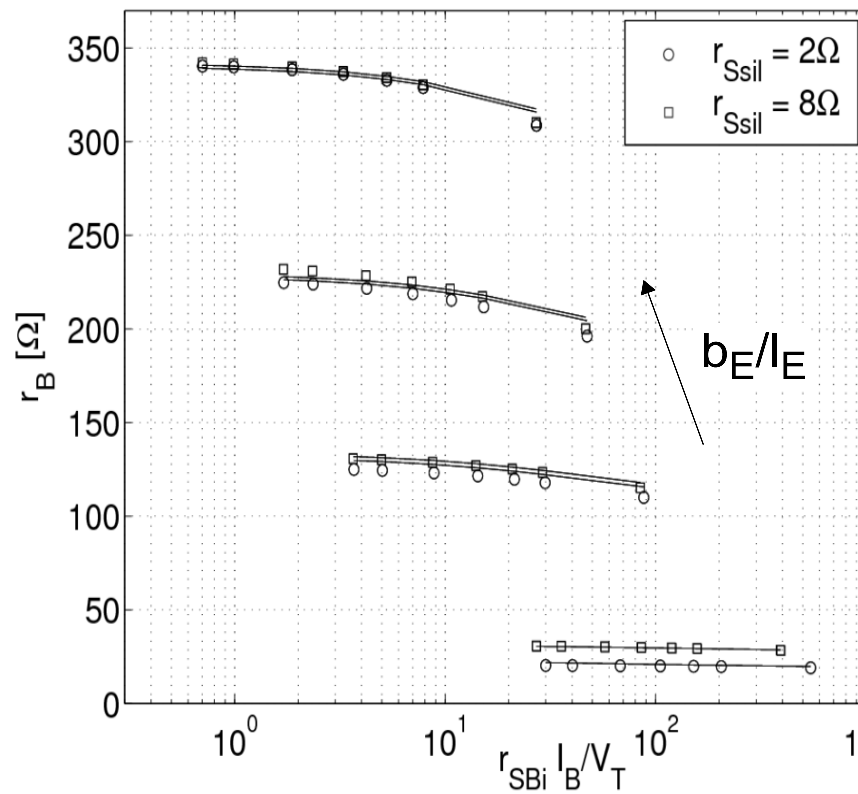
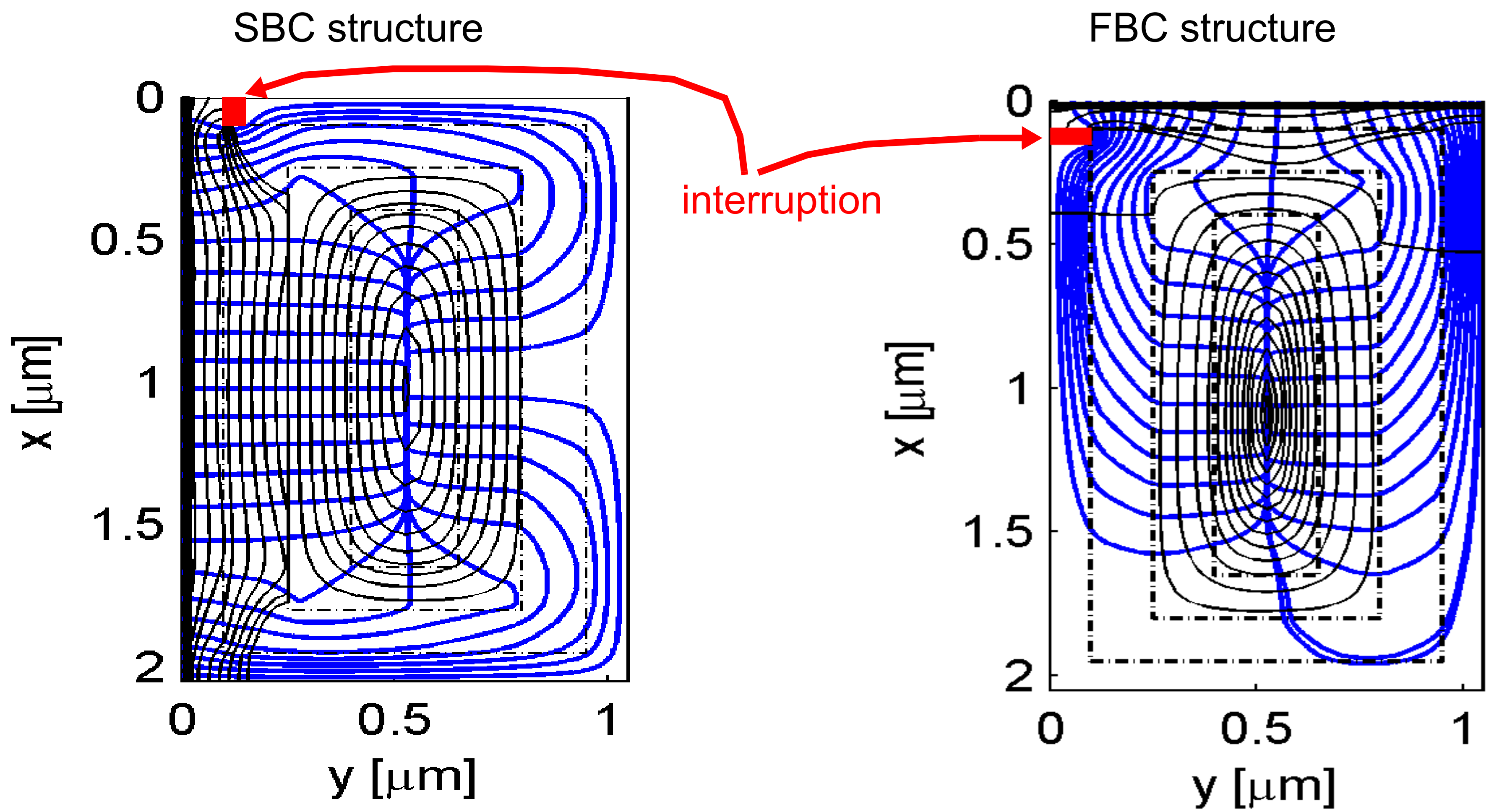


=> impact of emitter current crowding

⇒ good agreement up to long stripes ($b_E/l_E \geq 0.05$)

Impact of process issues: "broken" silicide



r_B = 148.5Ω (148Ω) r_B = 160Ω (148Ω)

⇒ little impact on SBC structure, around 10% for longer FBC structures

Conclusions

- updated set of layout dependent equations
  - single and double base contacts in parallel to the emitter
  - improved BE spacer resistance, especially for short transistors
  - variations of dimensions and silicide sheet resistance
  - negligible impact of vias (vs. slot contact)
  - proof of partitioning factor δ = 0.15 introduced in '91 paper
- new additional set of compact expressions for foreside base structures
  - single and double base
  - valid up to at least l_E = 10 b_E
- broken silicide has fairly little impact on DC base resistance

$\Rightarrow$ applicable to modern HBTs and BJTs

- For Details and equations see:
  M. Schroter, J. Krause, S. Lehmann, D. Celi, IEEE Trans. Electron Devices, 2008

