Construction of a Compact Modeling Platform and Its Application to the Development of Multi-Gate MOSFET Models for Circuit Simulation

M. Miura-Mattausch, H. J. Mattausch, H. Kikuchihara
Hiroshima University

M. Chan
Hong Kong University of Science & Technology

J. He
Peking University

H. Koike, T. Nakagawa
Advanced Industrial Science and Technology

Y. J. Park
Seoul National University

T. Tutsumi
Meiji University

Z. Yu
Tsinghua University

WCM, Boston, 2008

Background

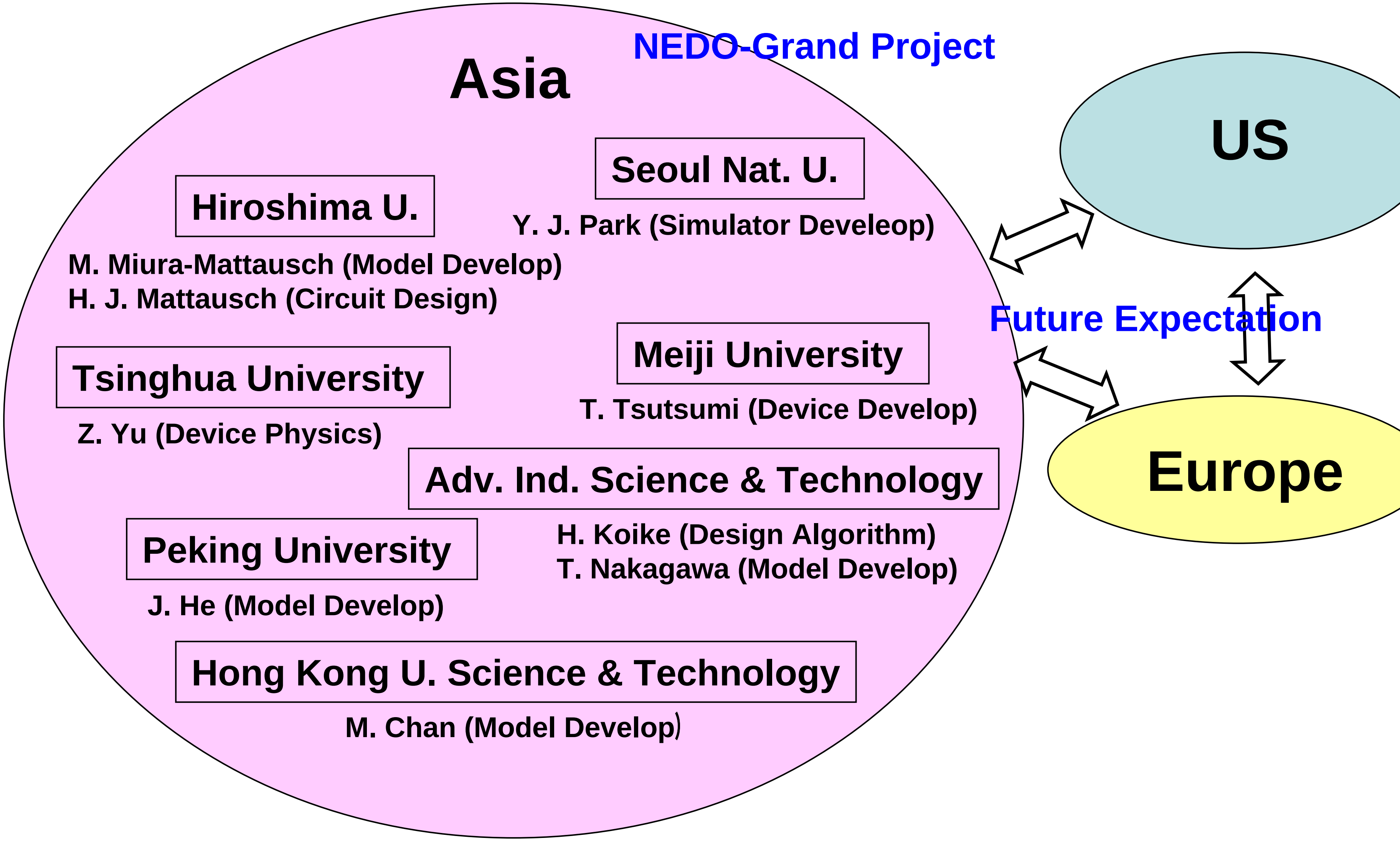
- ✓ Accurate compact models are highly required.
- ✓ Development of compact models takes time.
- ✓ Existing models describing individual device phenomena are not successfully utilized in compact models.
- ✓ Complete models are required to verify model elements.

Solution

- ● Cooperation among different research groups
- ● Provide a common modular platform enabling to merge different model components by plugging in modules

Establishment of International Cooperation

NDMI: Nano-Device Modeling Initiative



NEDO-Grand Project

Asia

Seoul Nat. U.

Y. J. Park (Simulator Develeop)

Hiroshima U.

M. Miura-Mattausch (Model Develop)
H. J. Mattausch (Circuit Design)

Tsinghua University

Z. Yu (Device Physics)

Meiji University

T. Tsutsumi (Device Develop)

Adv. Ind. Science & Technology

H. Koike (Design Algorithm)
T. Nakagawa (Model Develop)

Peking University

J. He (Model Develop)

Hong Kong U. Science & Technology

M. Chan (Model Develop)

US

Future Expectation

Europe

Tasks

I. Platform:

- ✓ Provide a Verilog-A Platform
- ✓ Provide a Prototype of Modules

II. Included Multi-Gate MOSFET Modules:

- ✓ Quantum Carrier Transport
- ✓ Mobility Model and Ballistic Effect
- ✓ Potential Solver
- ✓ Parasitic Effects

Subjects

Ⅰ. 1. Platform for Model Development

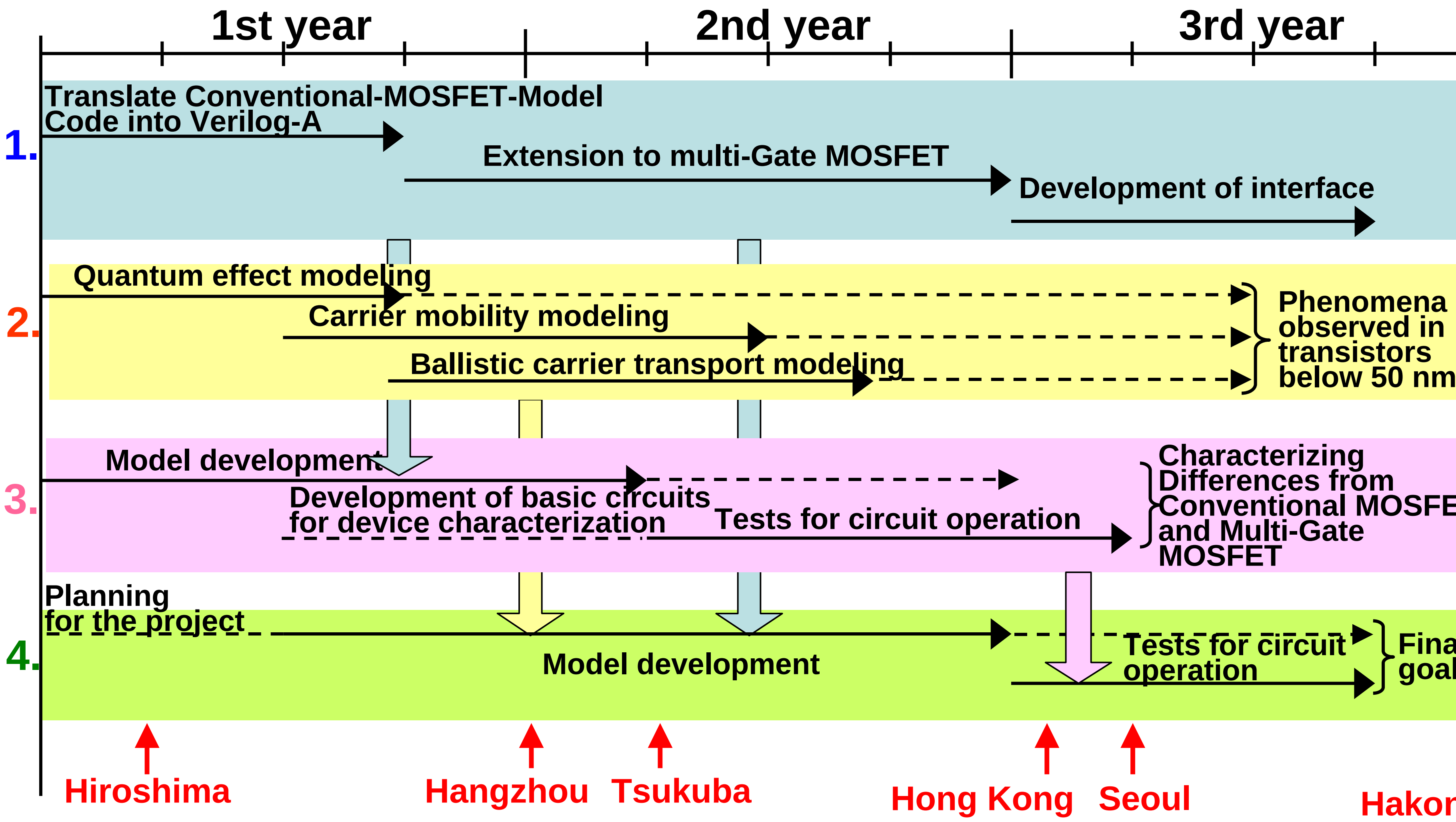
Ⅱ. MG-MOSFET Model Development with the Platform

2. Microscopic-Phenomena Modeling

3. SOI-MOSFET Modeling

4. MG-MOSFET Modeling

Development Schedule



1st year
2nd year
3rd year

1.
Translate Conventional-MOSFET-Model Code into Verilog-A
Extension to multi-Gate MOSFET
Development of interface

2.
Quantum effect modeling
Carrier mobility modeling
Ballistic carrier transport modeling
Phenomena observed in transistors below 50 nm

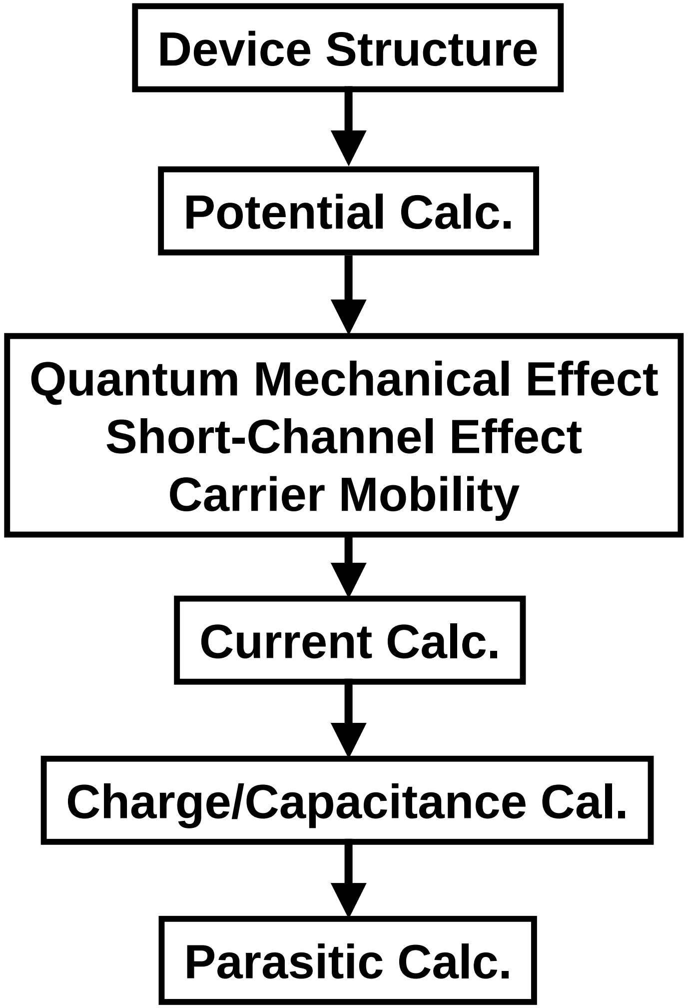
3.
Model development
Development of basic circuits for device characterization
Tests for circuit operation
Characterizing Differences from Conventional MOSFE
and Multi-Gate MOSFET

4.
Planning for the project
Model development
Tests for circuit operation
Fina
goal

Hiroshima
Hangzhou
Tsukuba
Hong Kong
Seoul
Hakor

Modularization

[Conventional Model Construction]



Device Structure

Potential Calc.

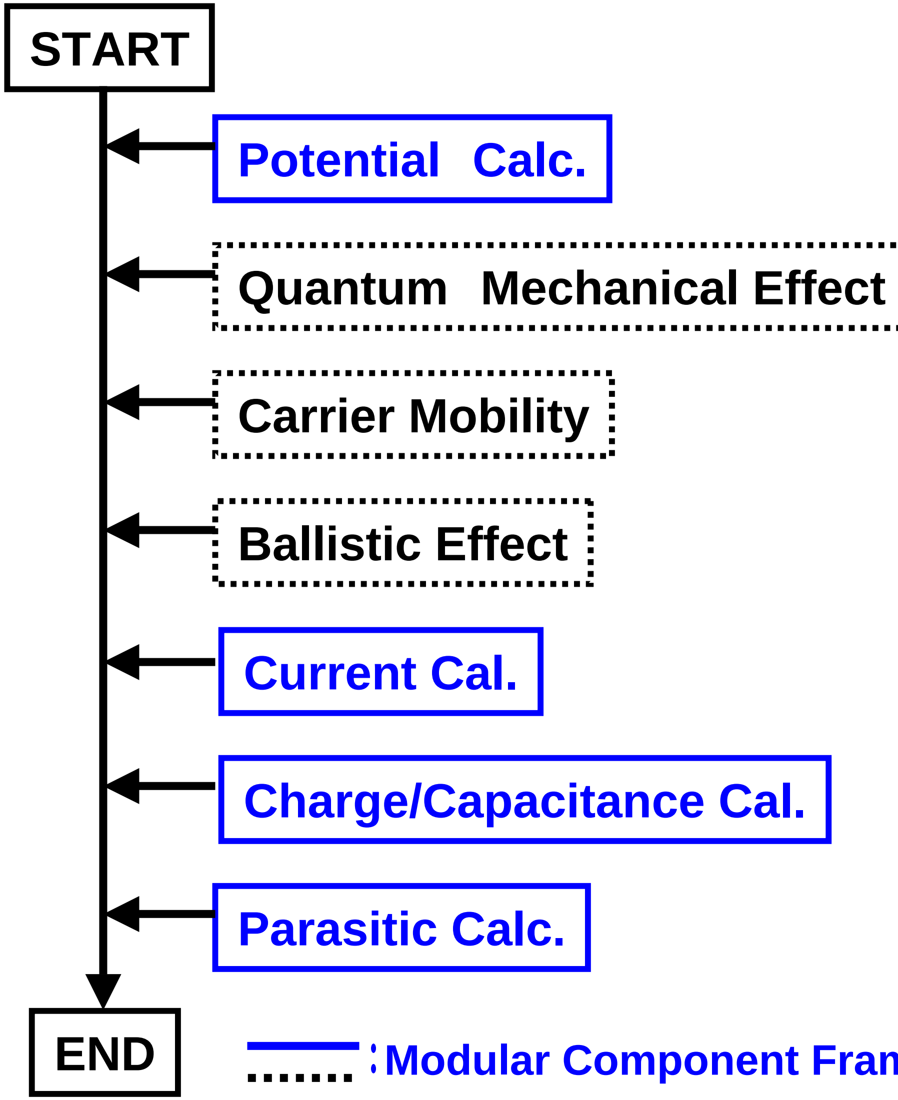
Quantum Mechanical Effect
Short-Channel Effect
Carrier Mobility

Current Calc.

Charge/Capacitance Cal.

Parasitic Calc.

[Our Proposal]



START

Potential Calc.

Quantum Mechanical Effect

Carrier Mobility

Ballistic Effect

Current Cal.

Charge/Capacitance Cal.

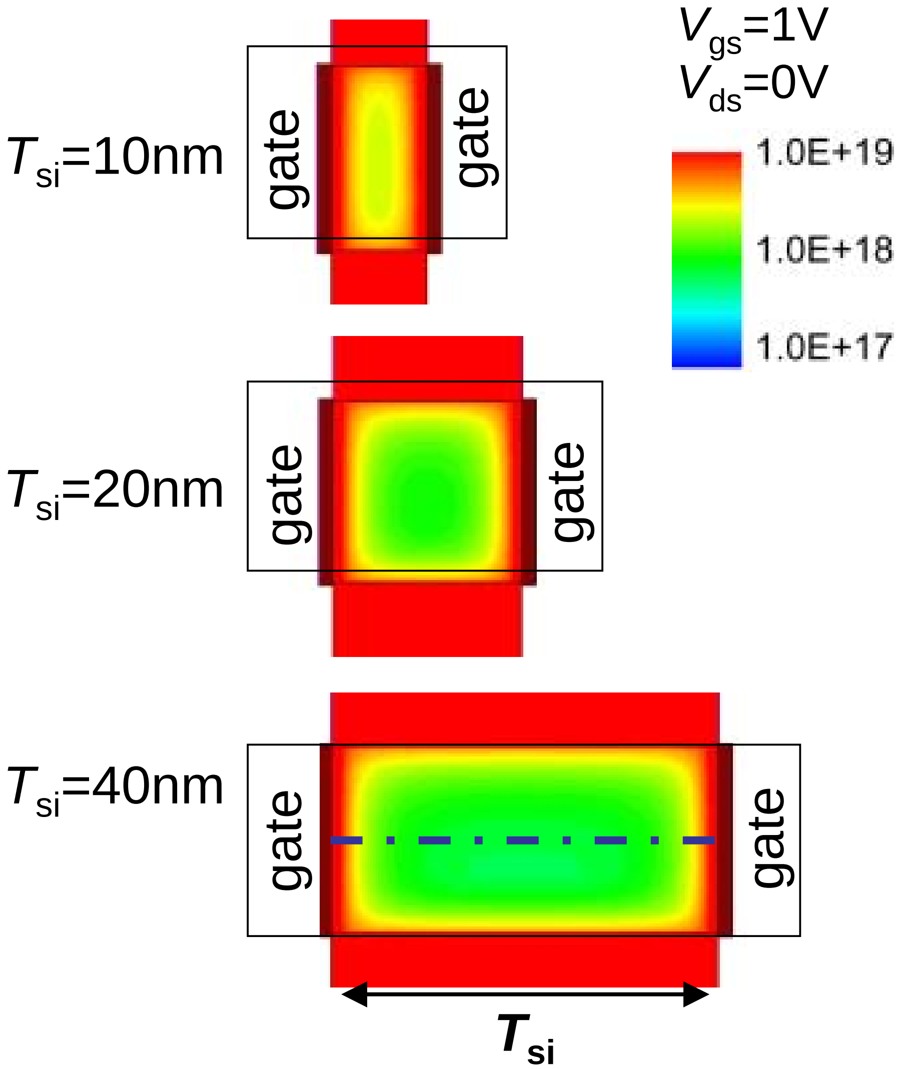
Parasitic Calc.

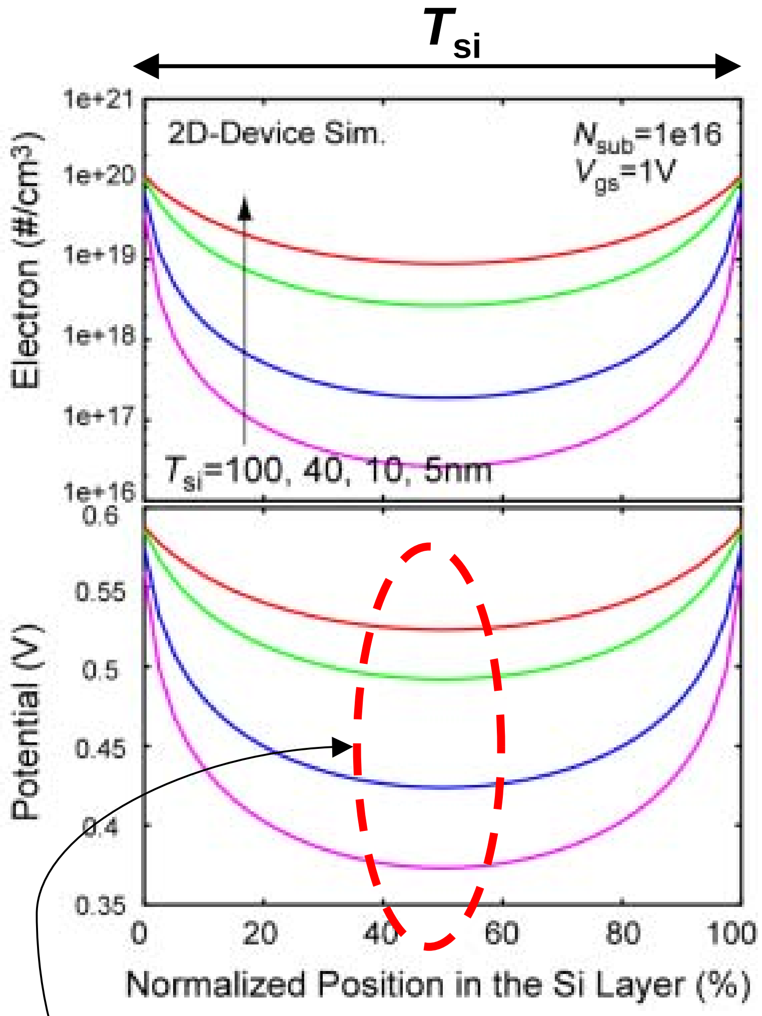
END

: Modular Component Fran

Specific Feature of MG-MOSFET

carrier concentration

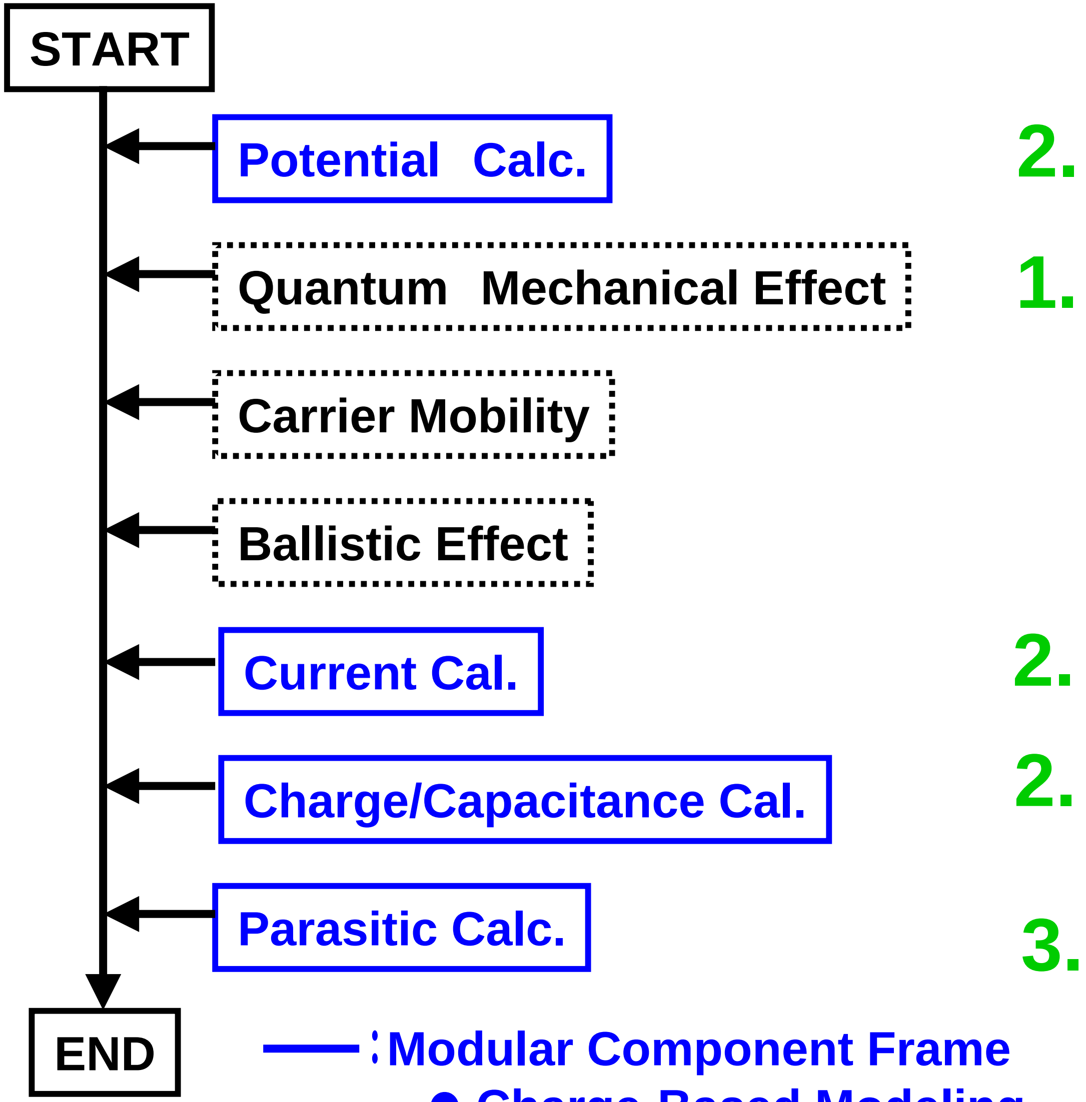




Body potential is floating.

The floating body potential makes modeling difficult.

Results Obtained



START

Potential Calc. 2.

Quantum Mechanical Effect 1.

Carrier Mobility

Ballistic Effect

Current Cal. 2.

Charge/Capacitance Cal. 2.

Parasitic Calc. 3.

END

—— : Modular Component Frame

- Charge-Based Modeling
- Potential-Based Modeling

1. Quantum Mechanical Effect

1-D Poisson's equation:

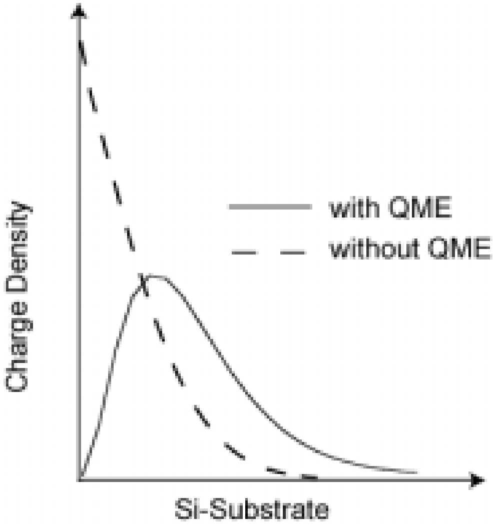
$$\frac{d^2\phi(x)}{dx^2} = \frac{q}{\varepsilon_{\mathrm{si}}}[N_a + n(x)]$$

[Classical Method]

$$n(x) = n_i \exp[q(\phi(x) - \phi_{Fn})/kT]$$

Yuan Taur, Jin He

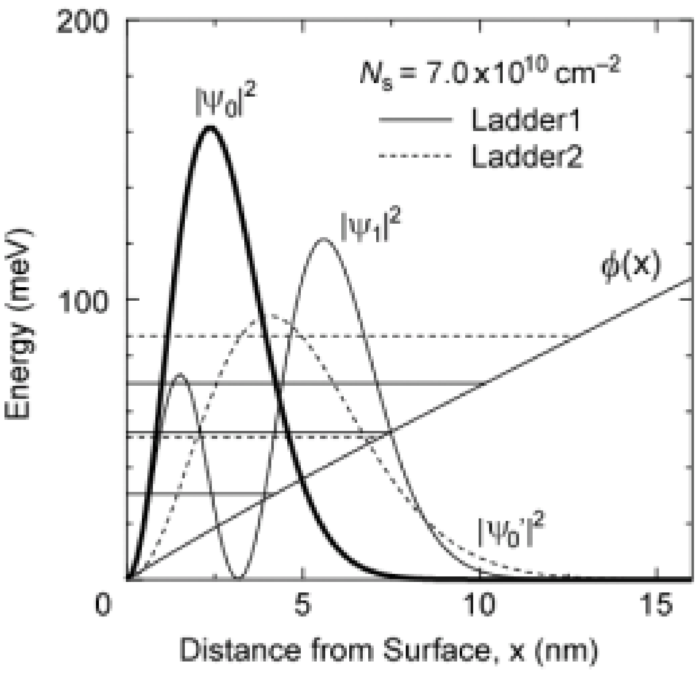
- Charge based and surface potential based
- Undoped channel



[Quantum Method]

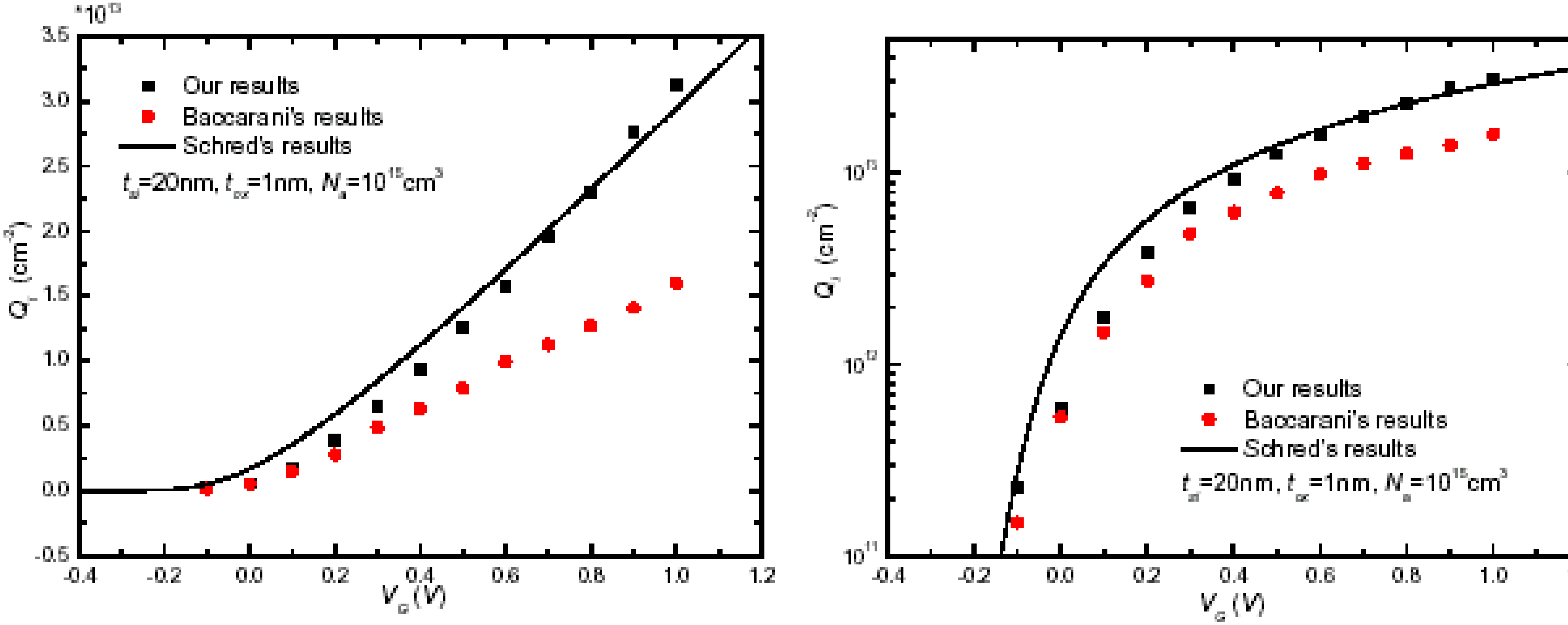
$$n(x) = \sum_{n=1}^{N_t} \sum_{k=1}^{N_m} \left|\psi_{n,k}(x)\right|^2 N_k$$

$$\times \ln\{1 + \exp[-(E_{n,k} - E_{Fn})/kT]\}$$



Comparison of Inversion Charge Density vs. V_G

T_{si}=20nm

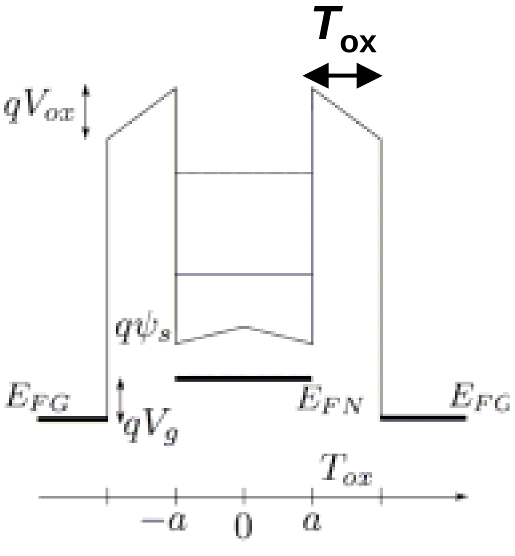


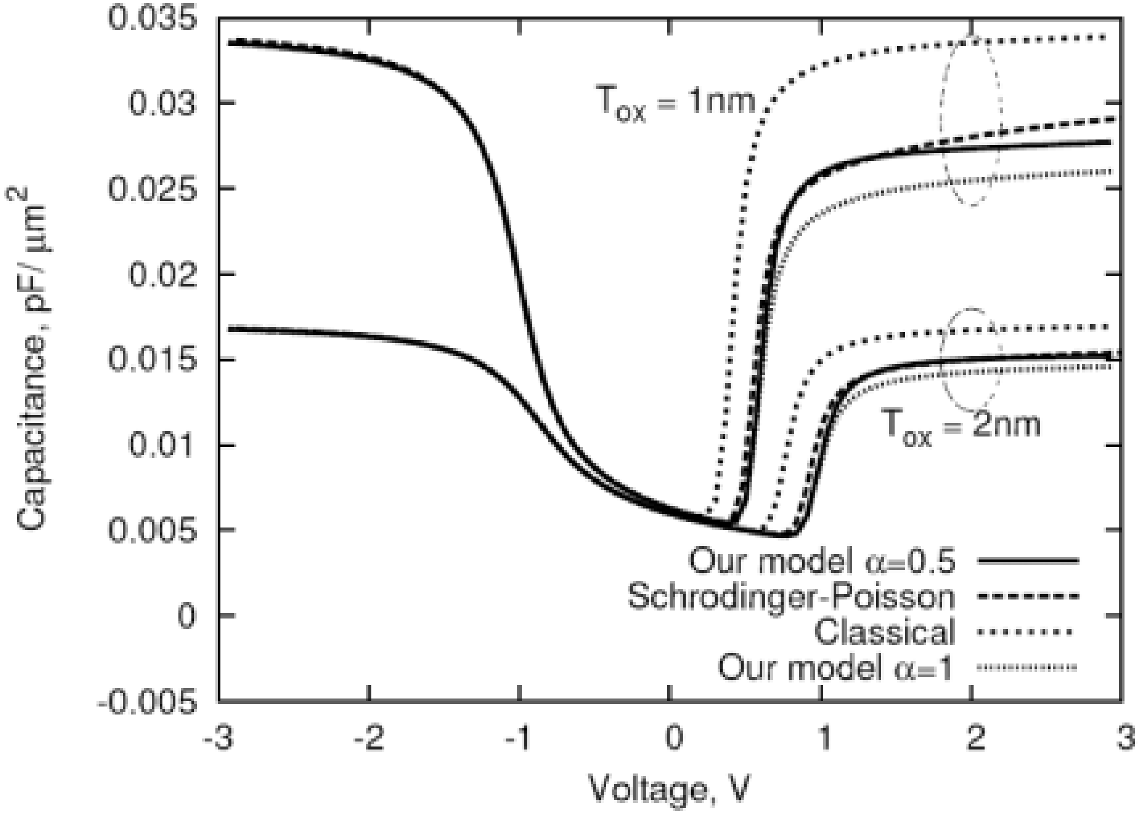
linear plot

log plot

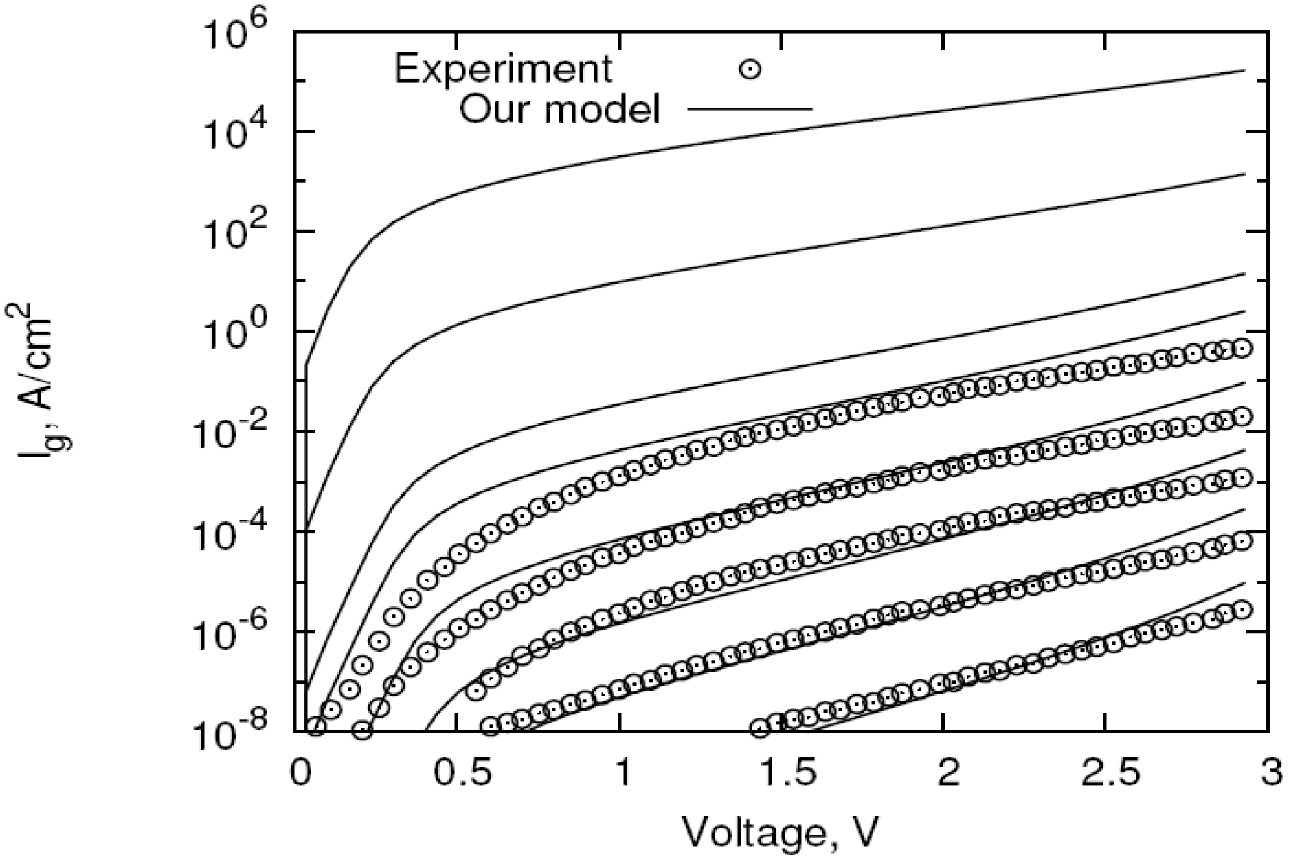
Comparison among our model, Baccarani’s model and Schred’s data

Influence of T_{ox} on Capacitance





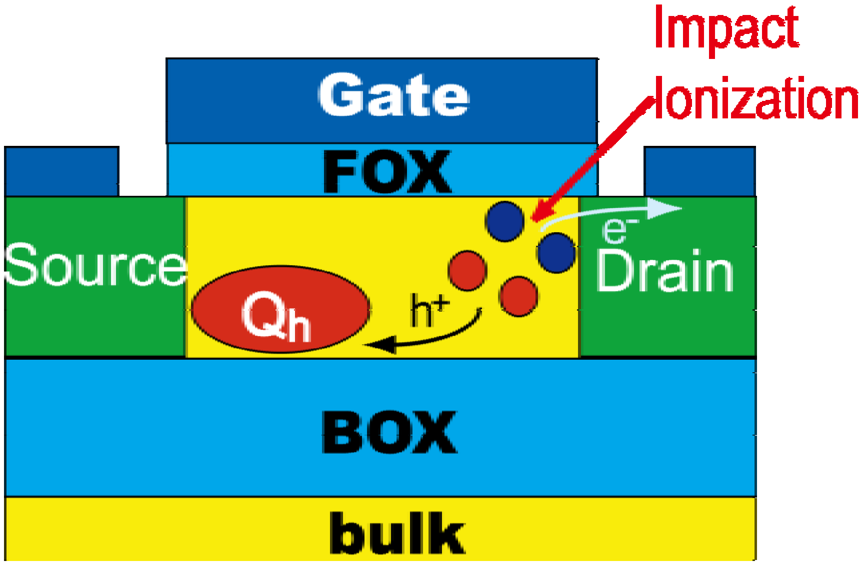
Influence of T_{ox} on Gate Tunneling Current

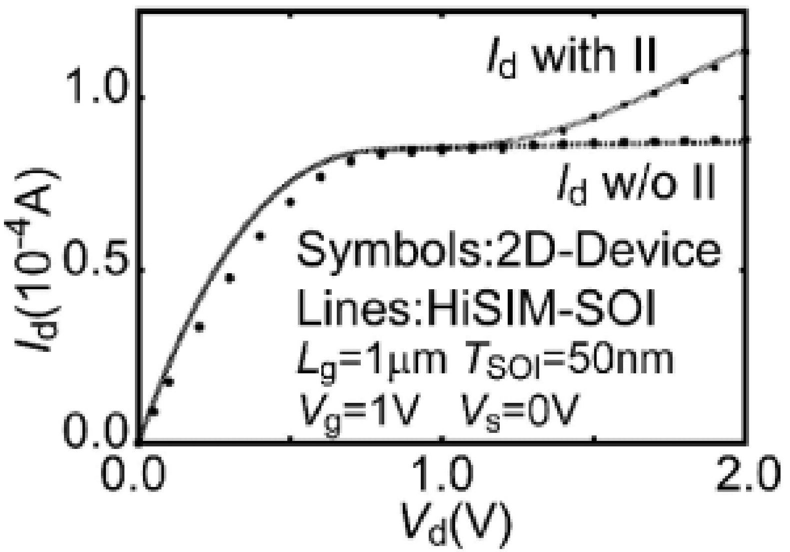


2. Potential, Current, Capacitance

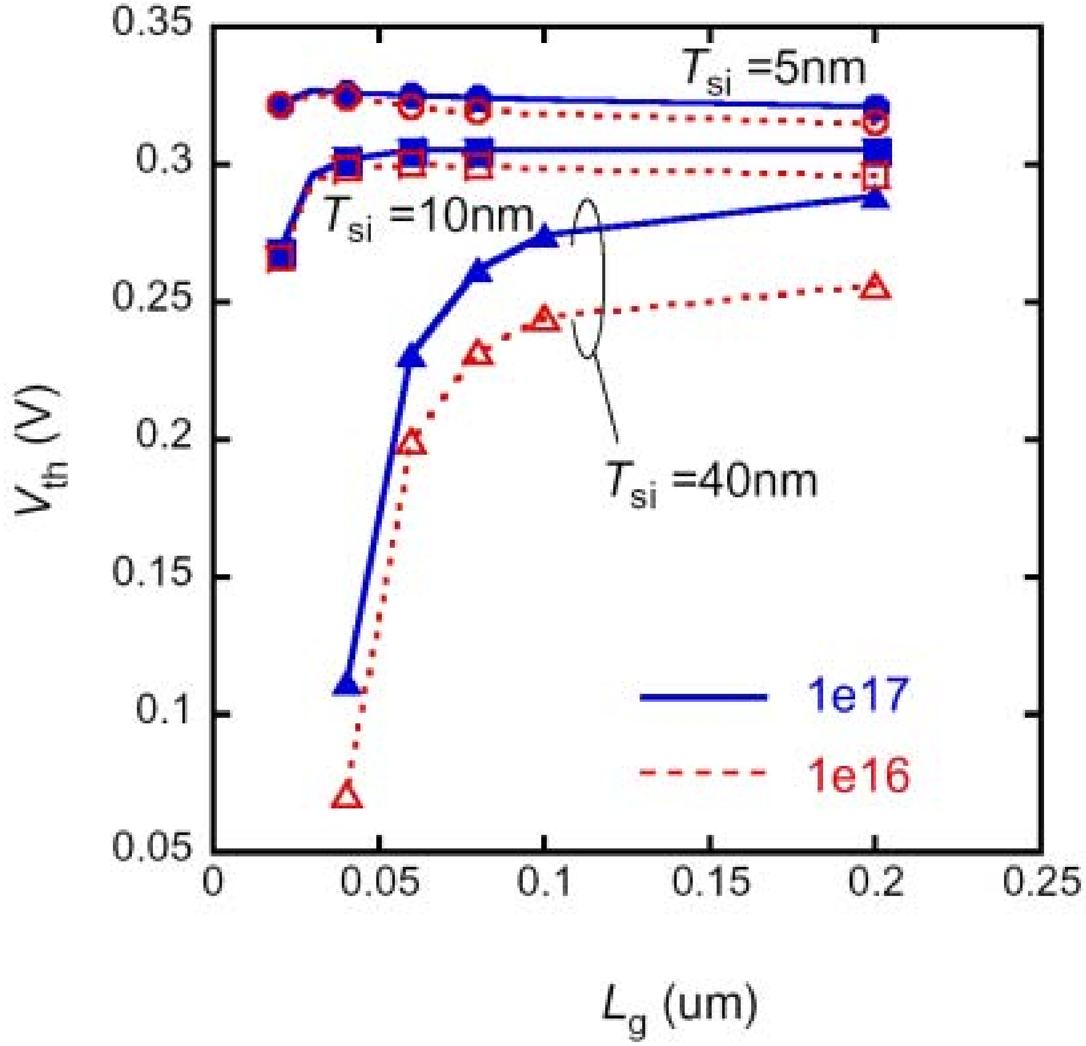
SOI-MOSFET

Modeling of Floating- Body Effect

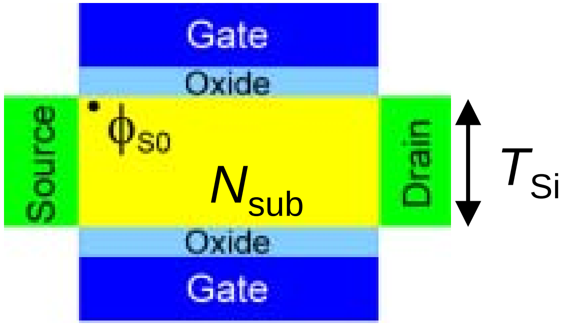


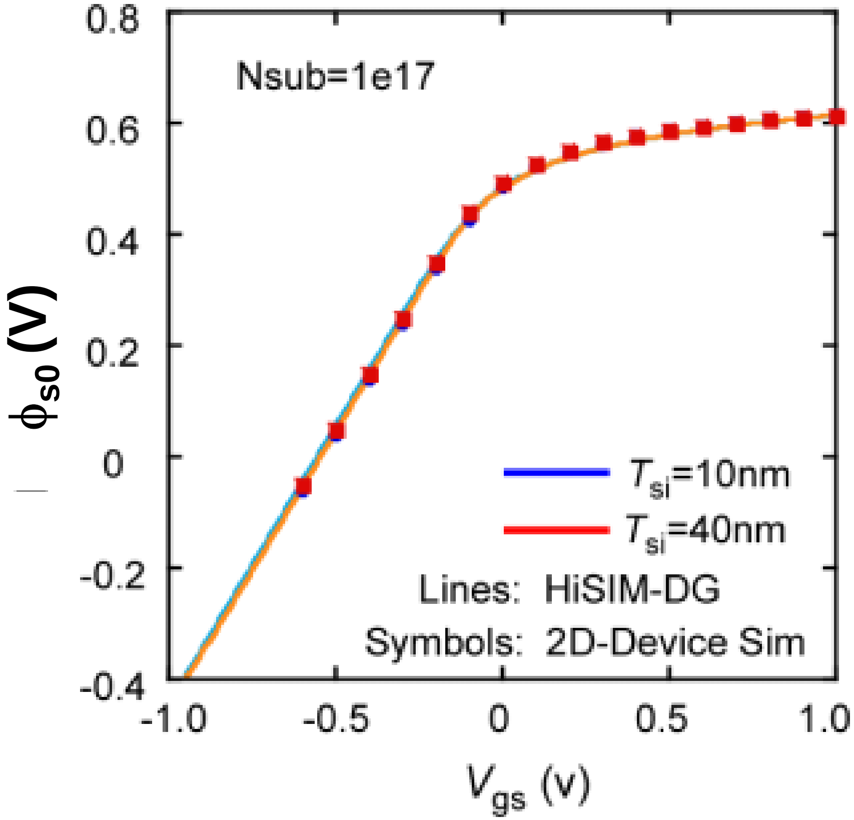


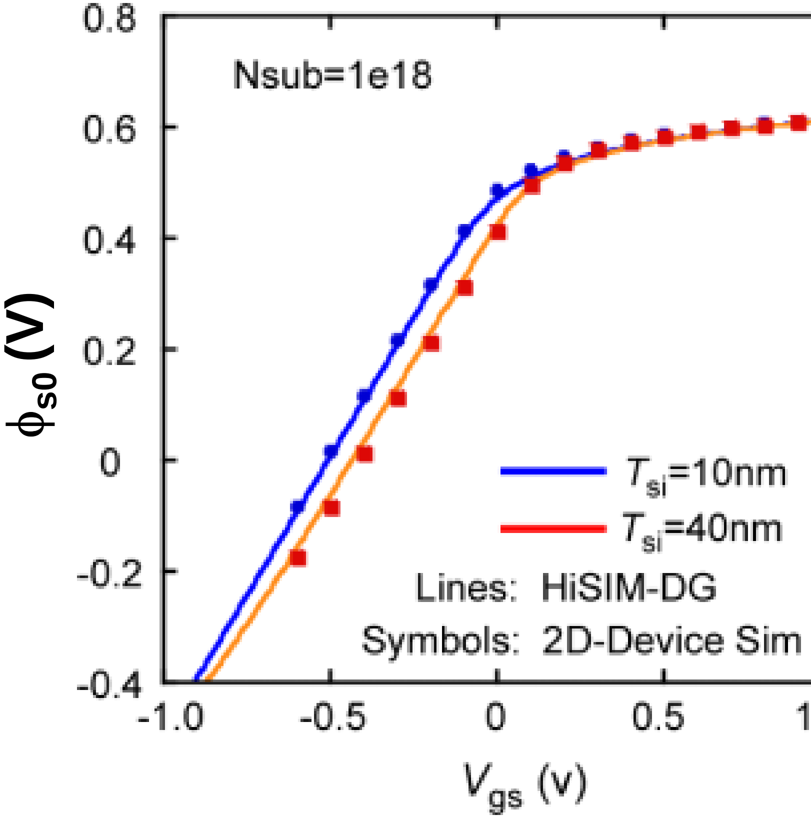
Short-Channel Effect in MG-MOSFET



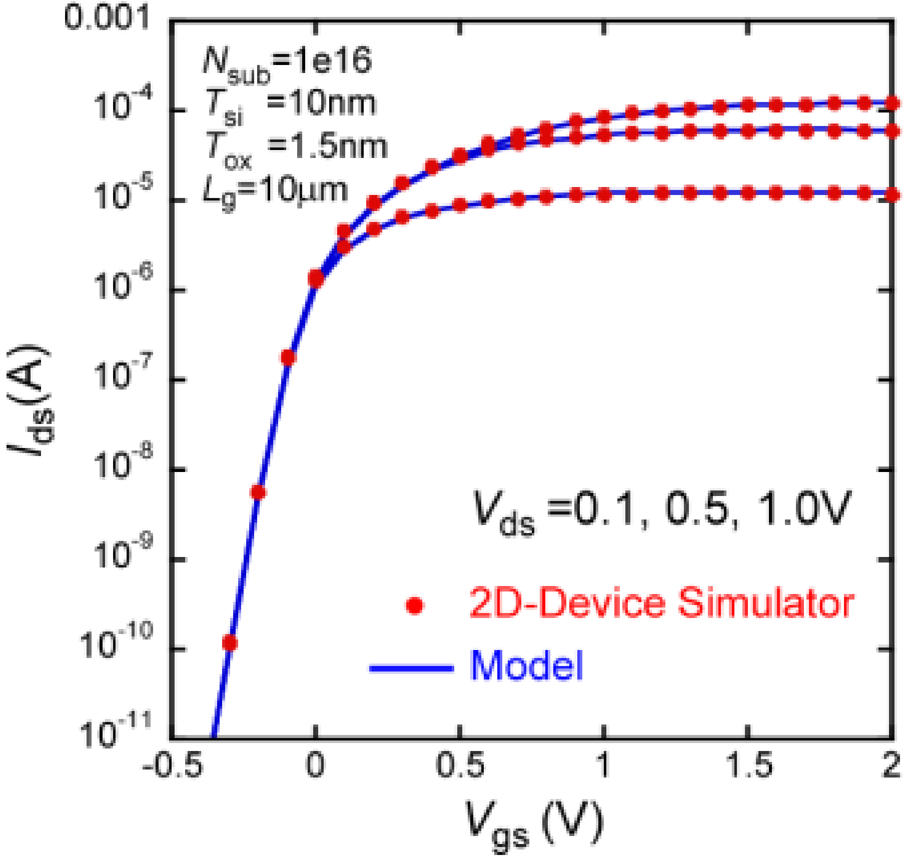
Comparison of Potential Dependency on T_{si} & N_{sub}

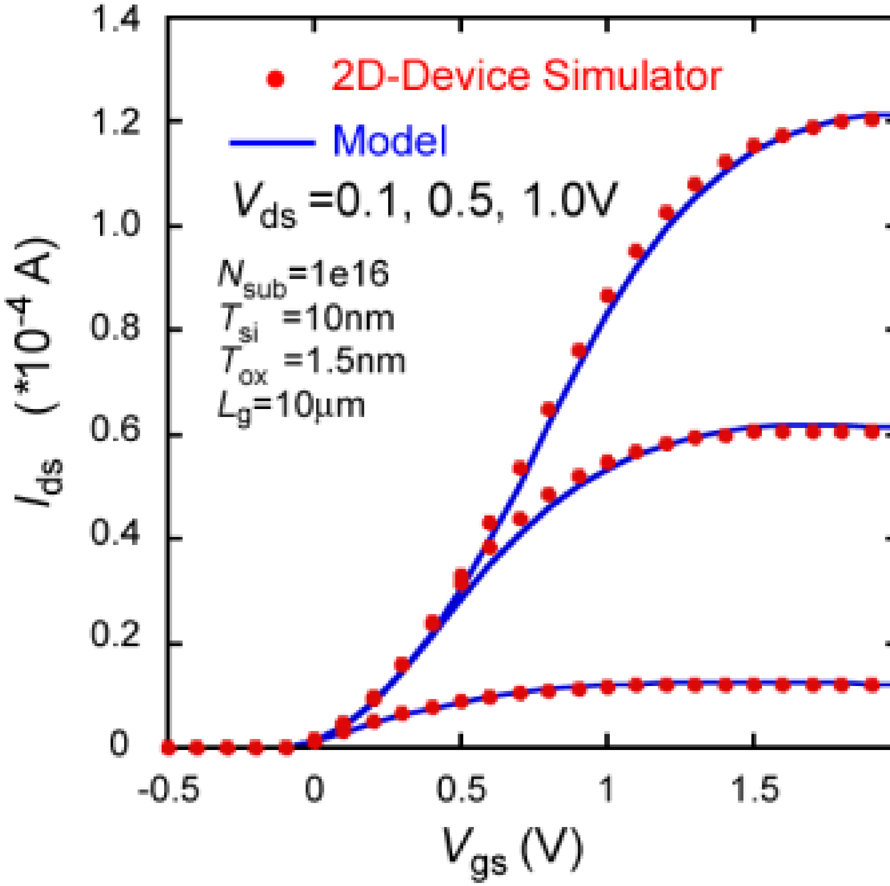




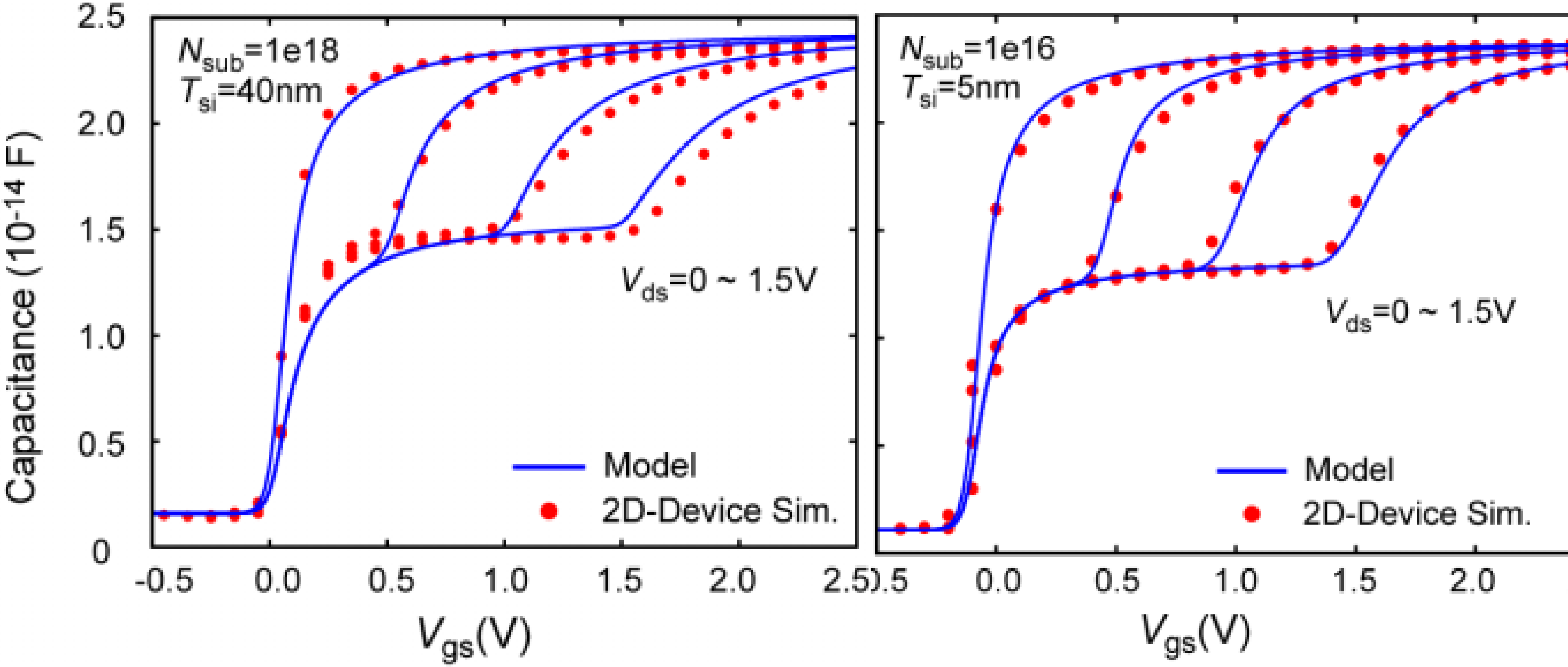


I_{ds}-V_{gs} Characteristics





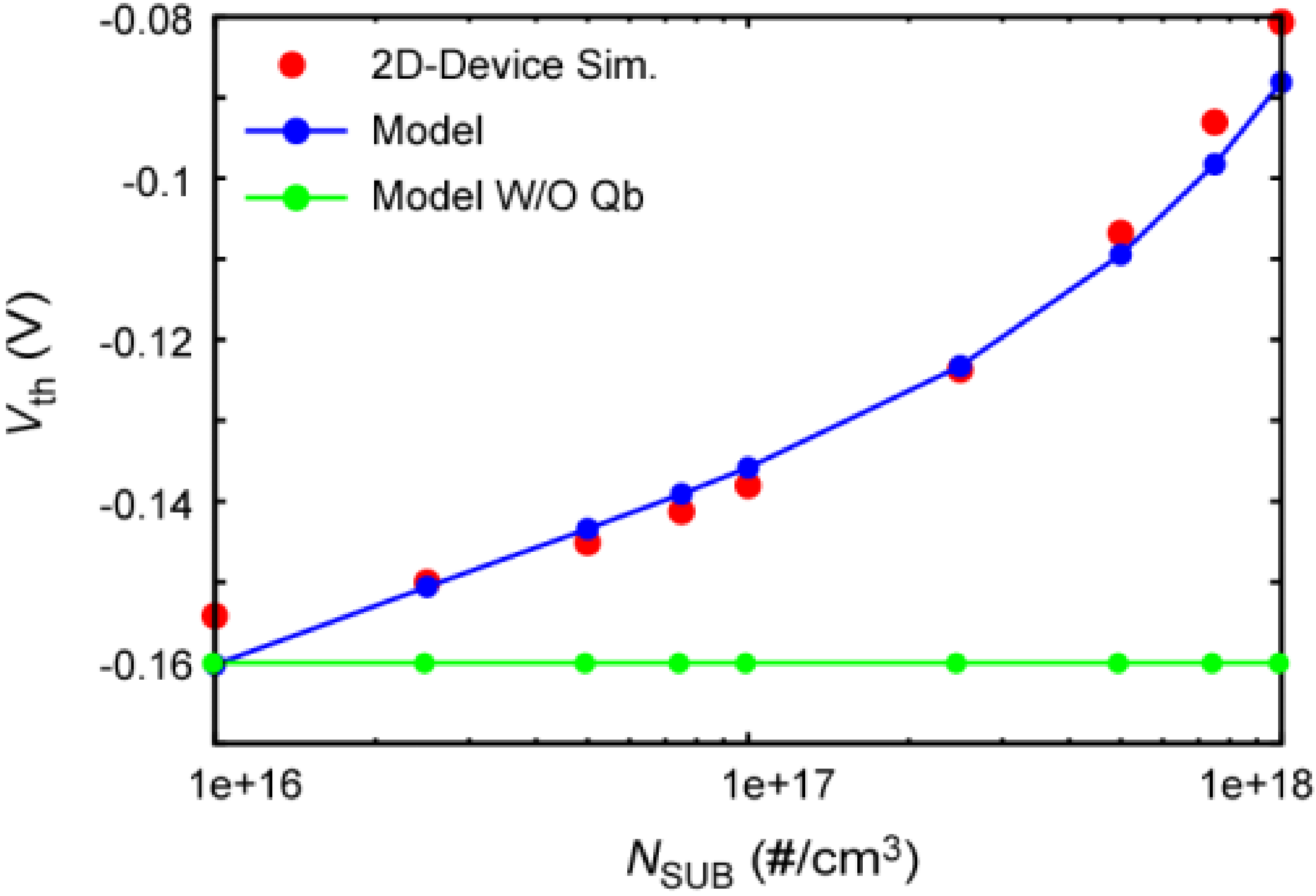
C-V Characteristics



Reduction of T_{si} gives small influence on the capacitance.

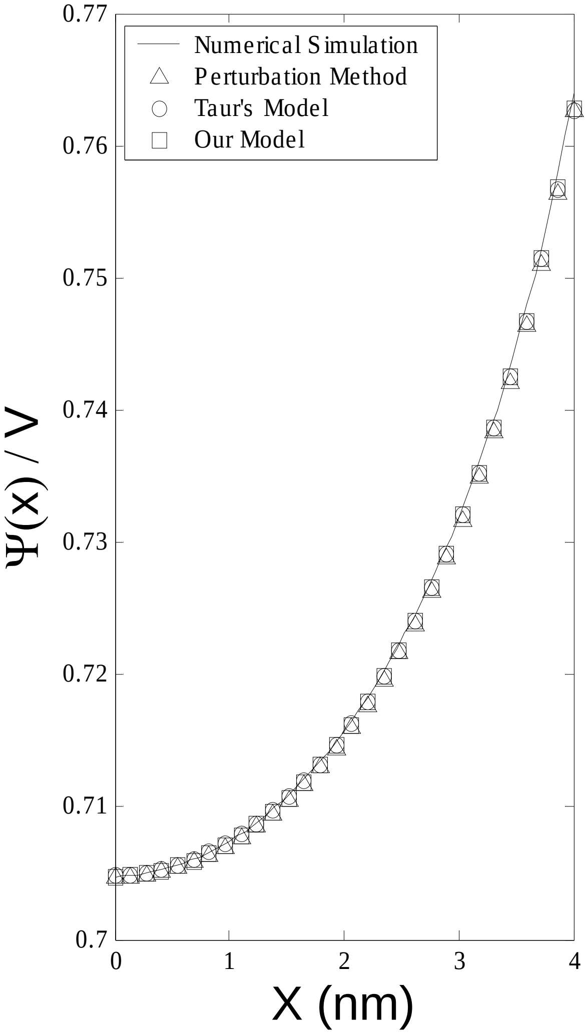
Impurity-Concentration Dependence of V_{th}

T_{SI}=10nm, T_{ox}=1nm, L_g=1um, V_{ds}=50mV

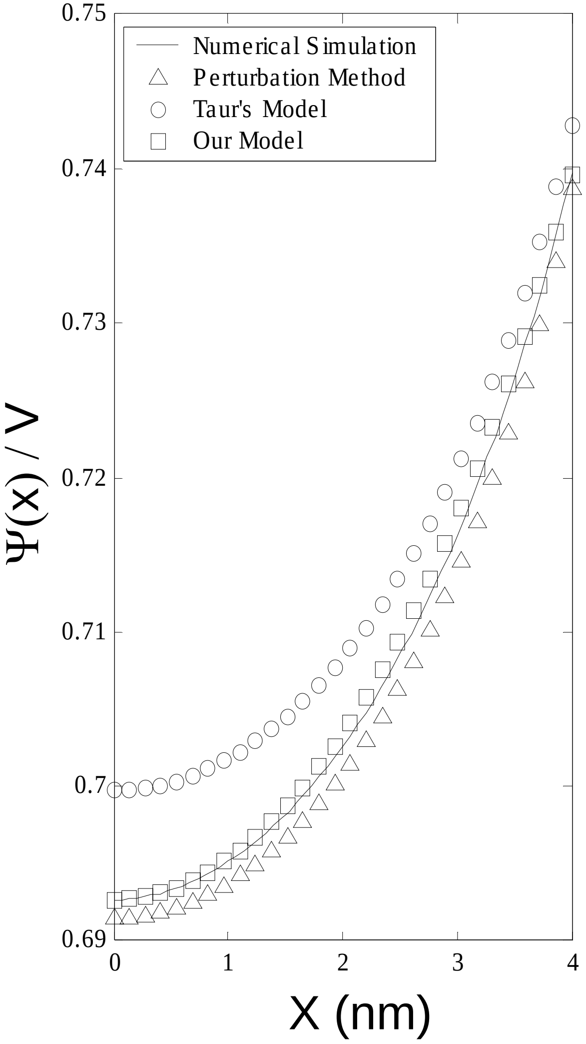


Influence of Q_b cannot be ignored.

Closed-Form Equation

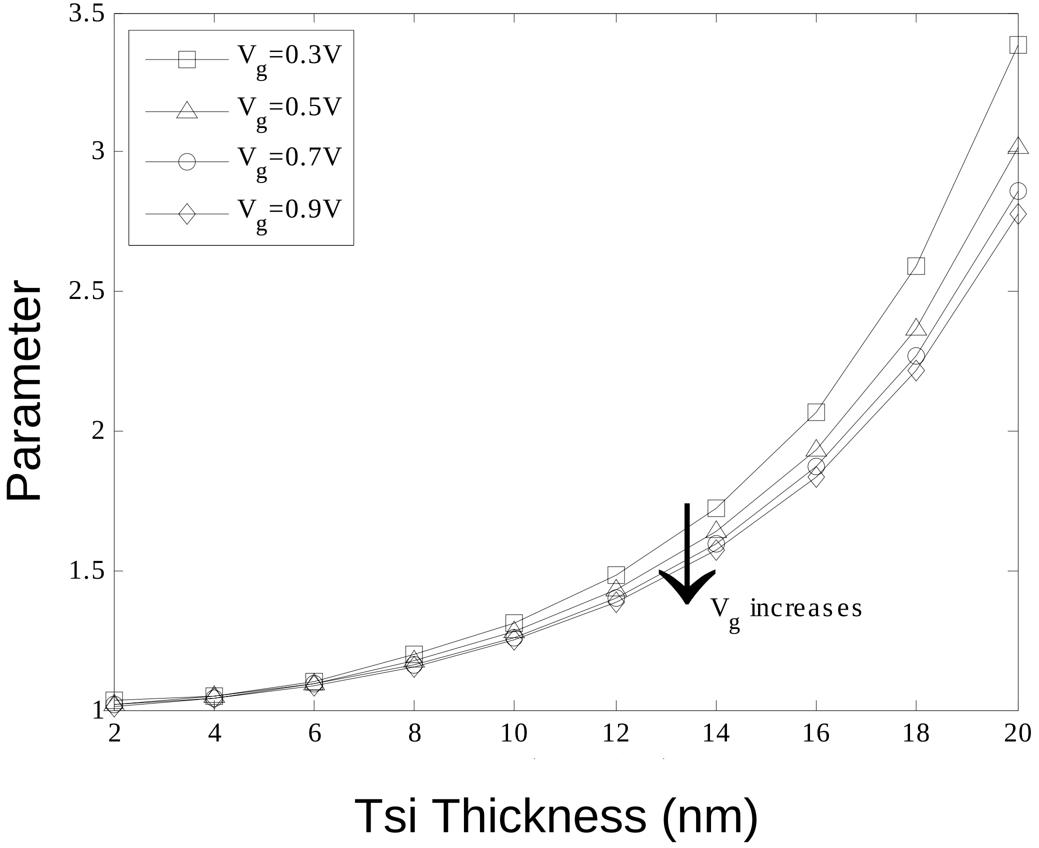


$N_A = 10^{16}\,\mathrm{cm}^{-3}$

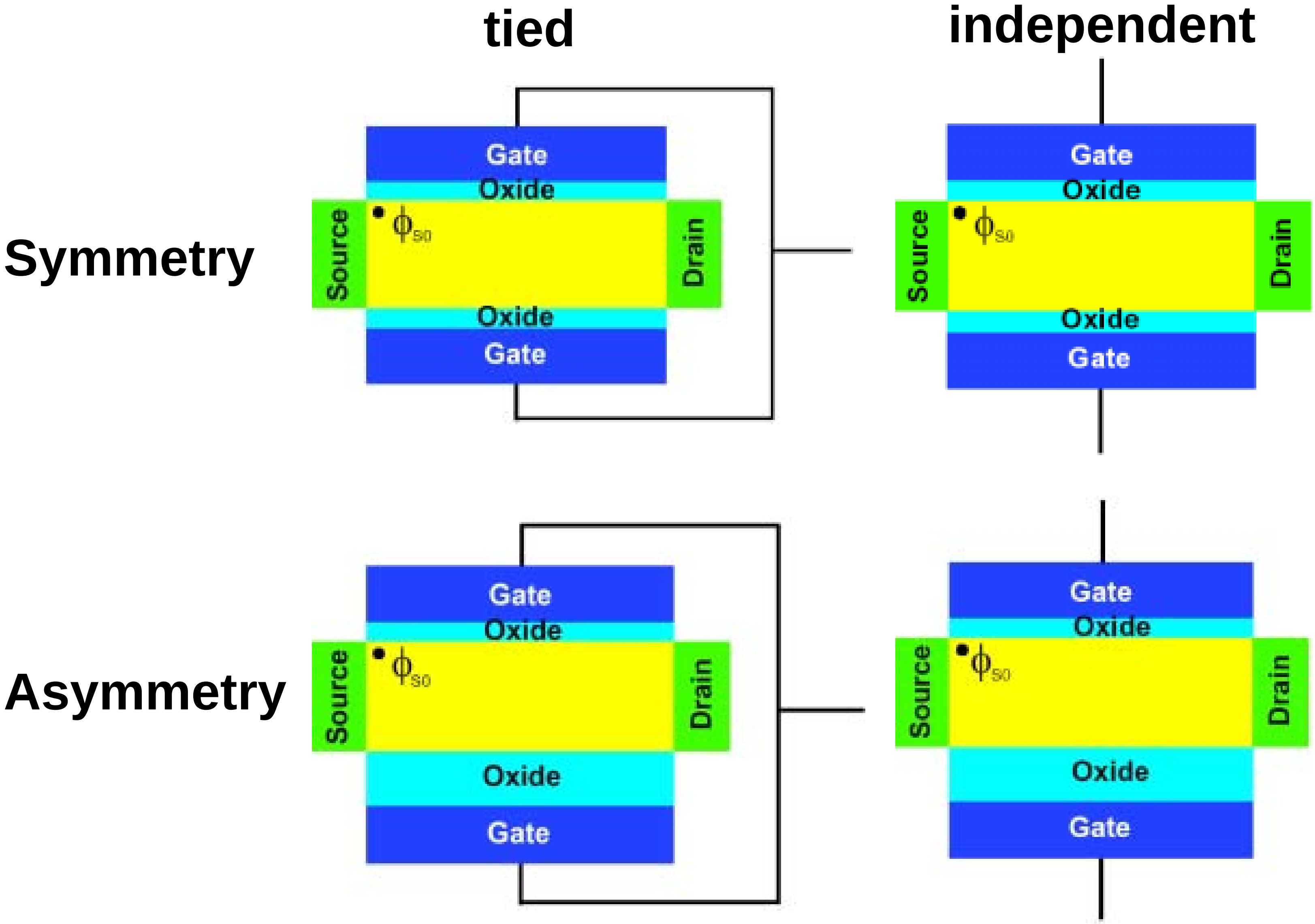


$N_A = 10^{18}\,\mathrm{cm}^{-3}$

Parameter Value Used in the Equation



Different Devices/Applications

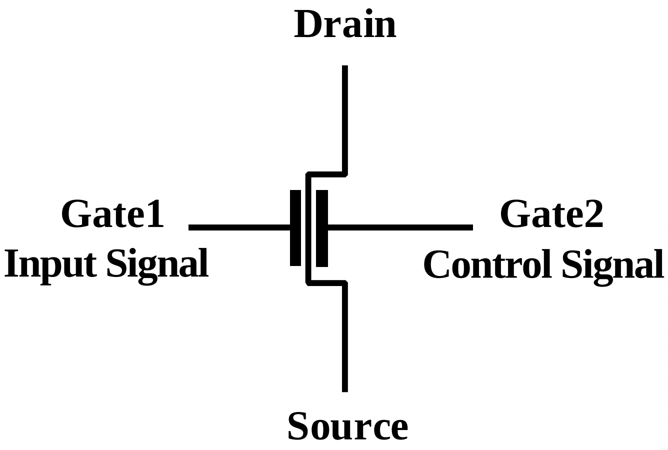

tied

independent

Symmetry

Asymmetry

I_{ds}-V_{g1}, V_{g2} Characteristics



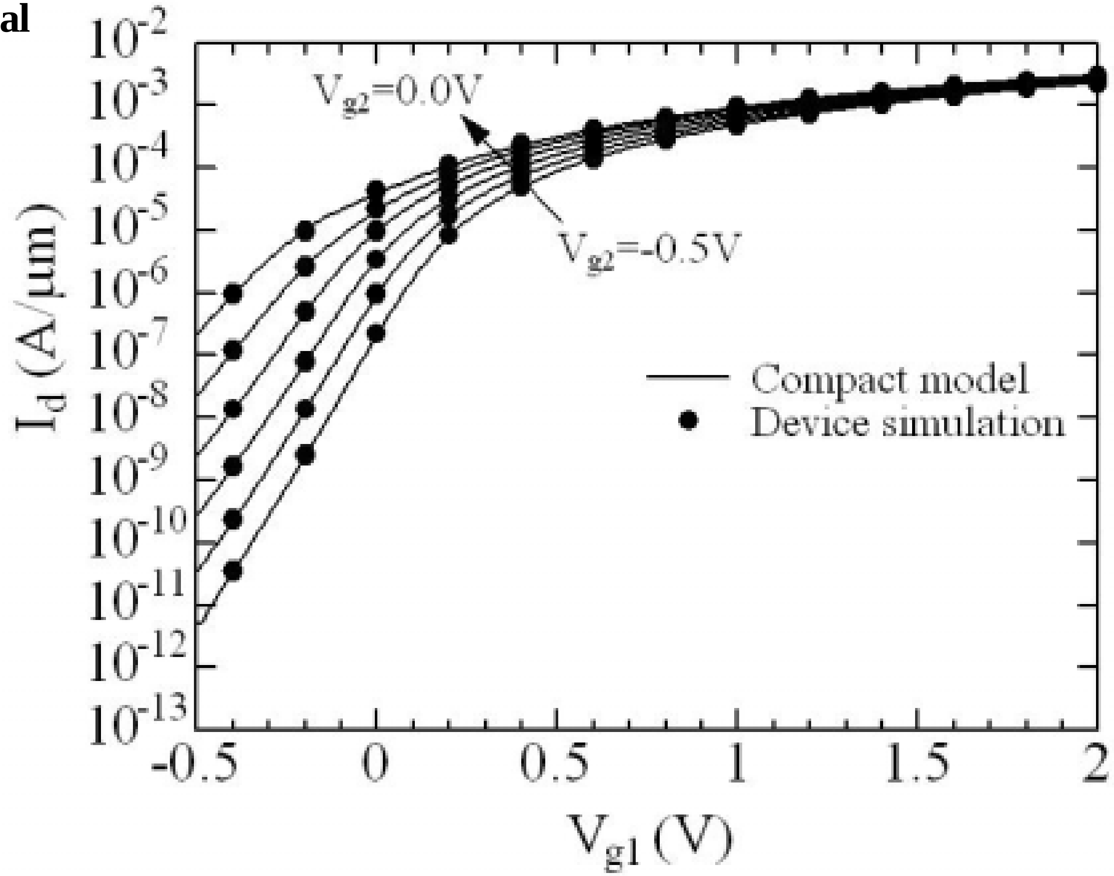
Drain

Gate1
Input Signal

Gate2
Control Signal

Source

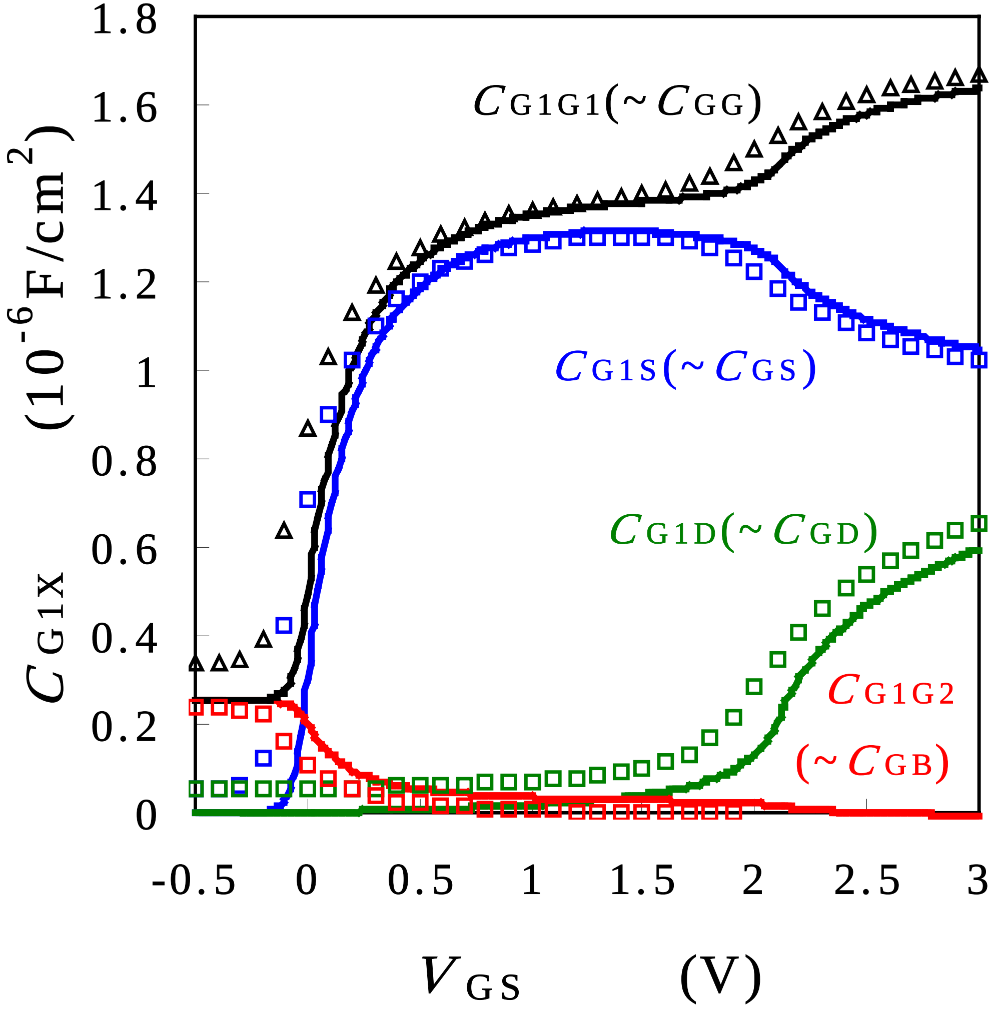
Symmetry, tied



UTB SOI-like DG MOSFET

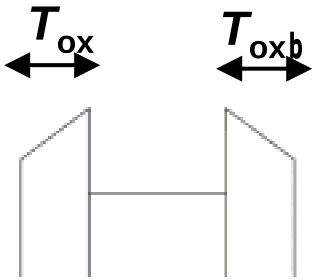
Asymmetry, independent

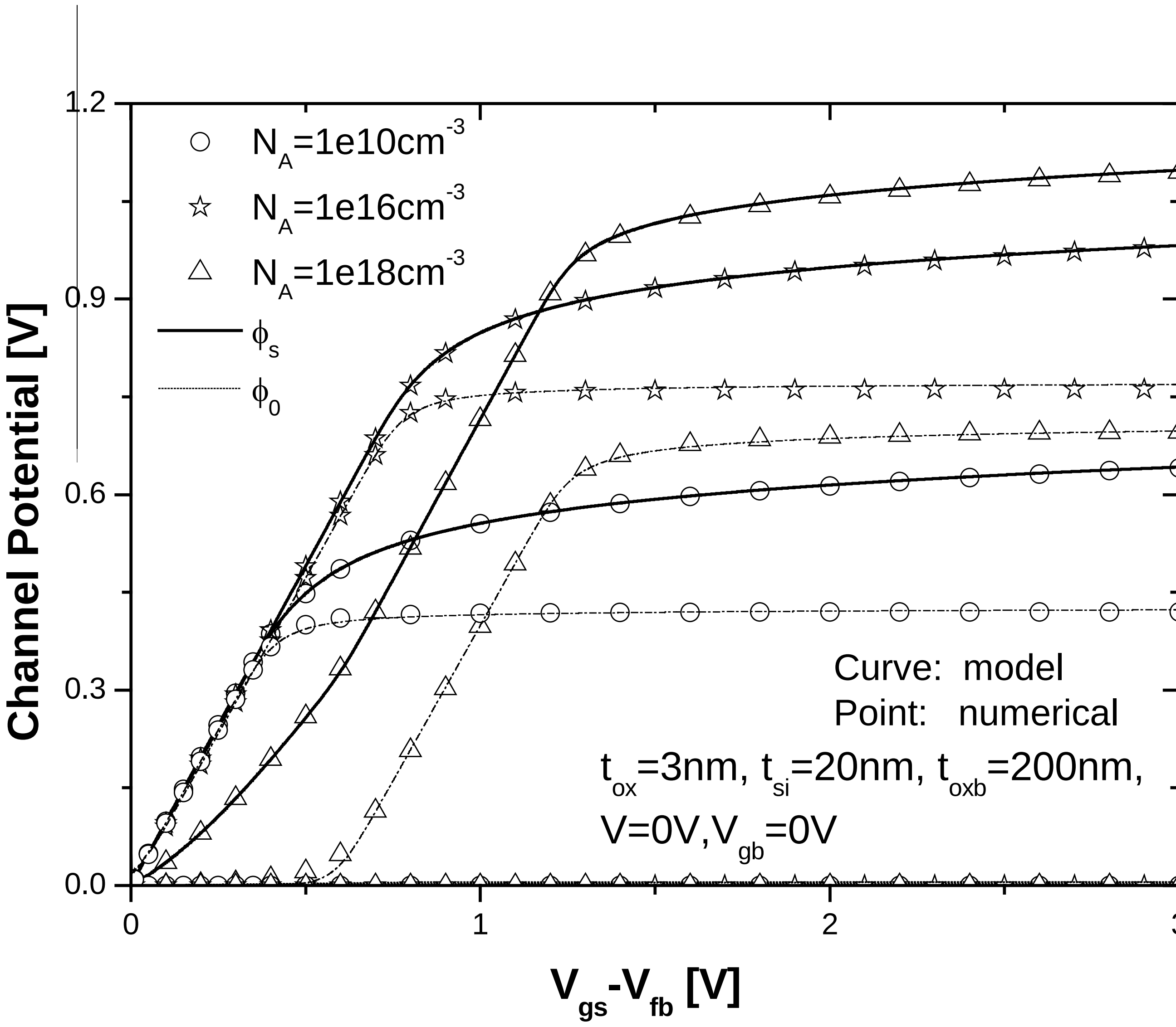
L_G= 200nm
T_{OX1}= 2nm, T_{OX2}= 10nm, T_{Si}= 5nm
V_{G2S}=-0.5V,V_{DS}=1.5V



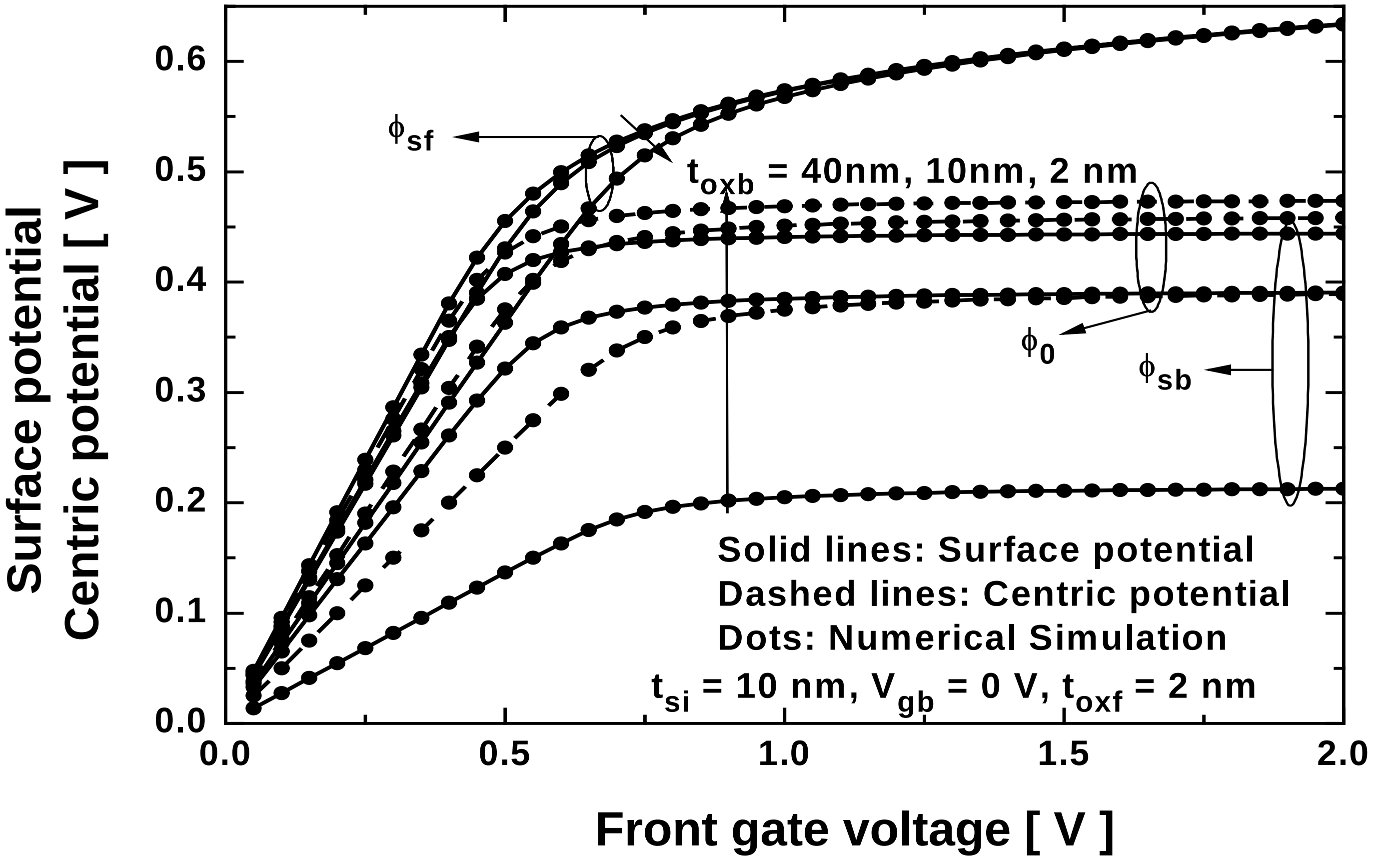
Marks: ATLAS simulation
Lines: Compact model

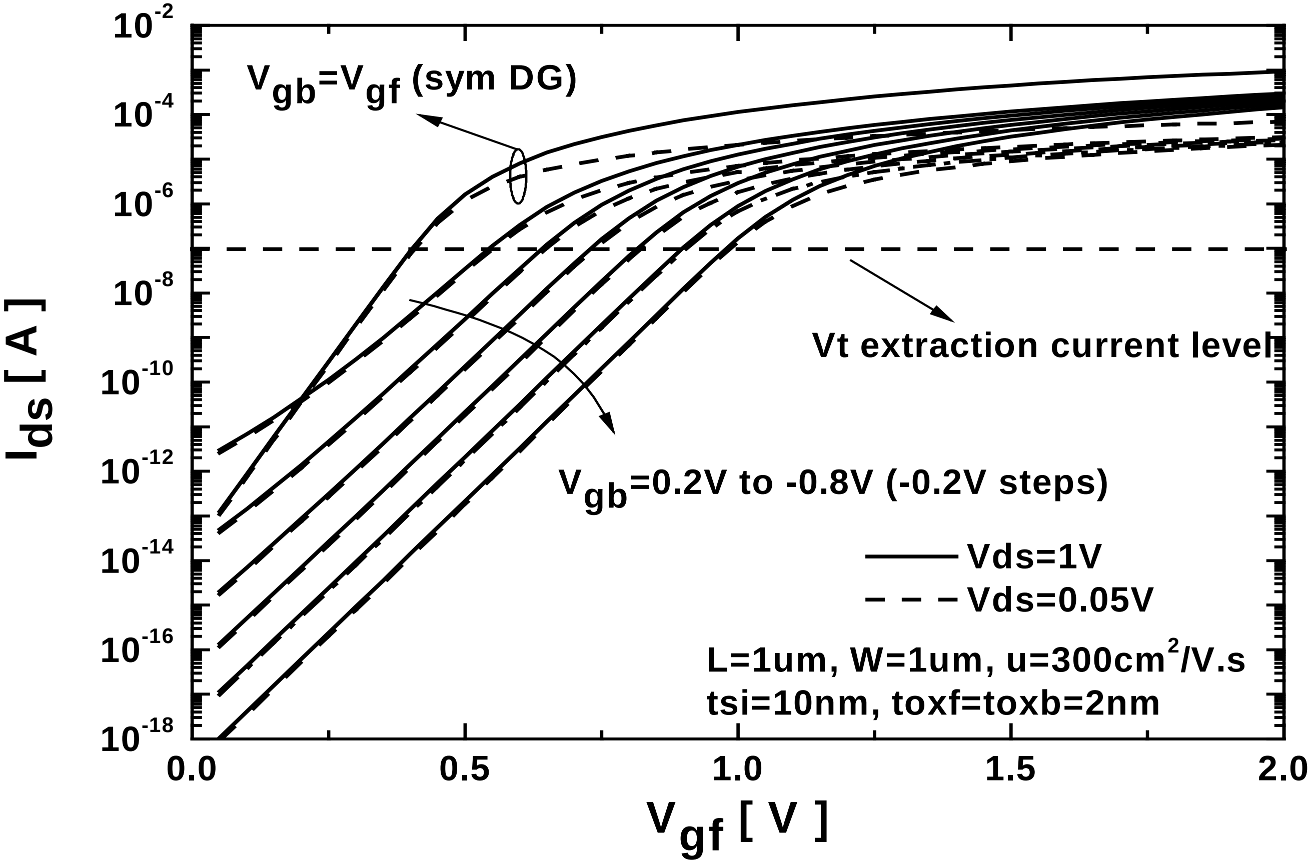
Asymmetry, independent



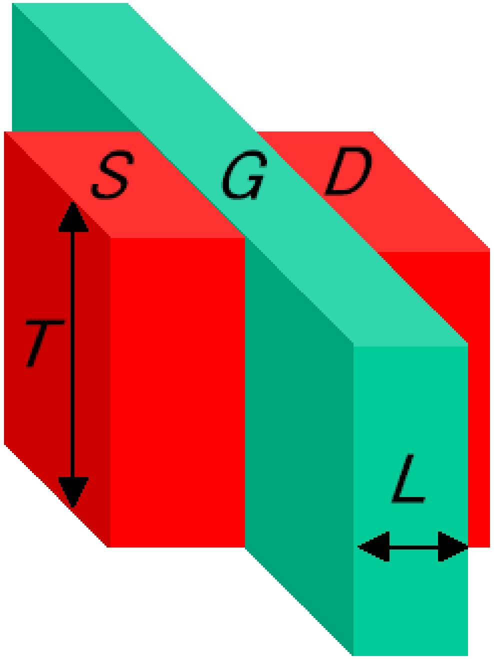


Surface potential & Centric potential v.s V_{gf}




$V_{gb}=V_{gf}$ (sym DG)
Vt extraction current level
V_{gb}=0.2V to -0.8V (-0.2V steps)
Vds=1V
Vds=0.05V
L=1um, W=1um, u=300cm^2/V.s
tsi=10nm, toxf=toxb=2nm
I_{ds} [A]
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
10^{-12}
10^{-14}
10^{-16}
10^{-18}
0.0
0.5
1.0
1.5
2.0
V_{gf} [V]

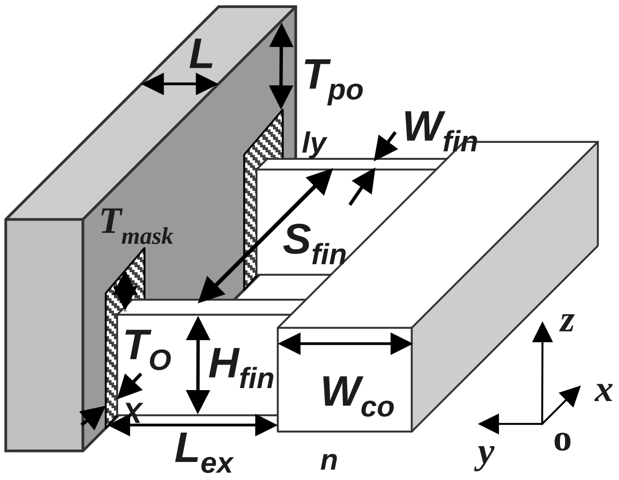
Device Fabrication



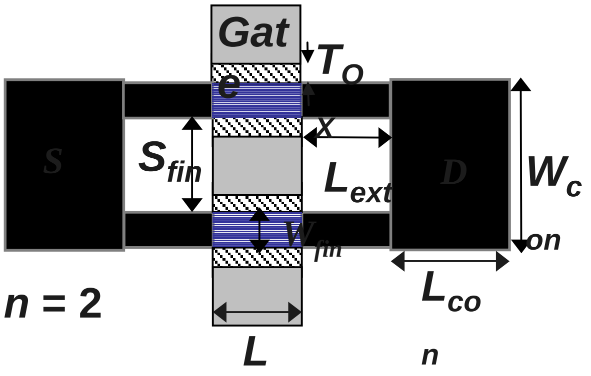
Various Device Sizes for Verifying Developed Models

3. Parasitic Capacitance

- **Consists of overlap (C_{ov}) and fringing (C_{fr}) capacitance**
- **Fringing capacitance can be further decomposed into outer fringing (C_{of}) and inner fringing (C_{if}) capacitance**
- **C_{if} capacitance is relative small in accumulation and strong inversion.**
- **As a MOSFET always operates at strong inversion at high frequency, C_{if} is ignored.**



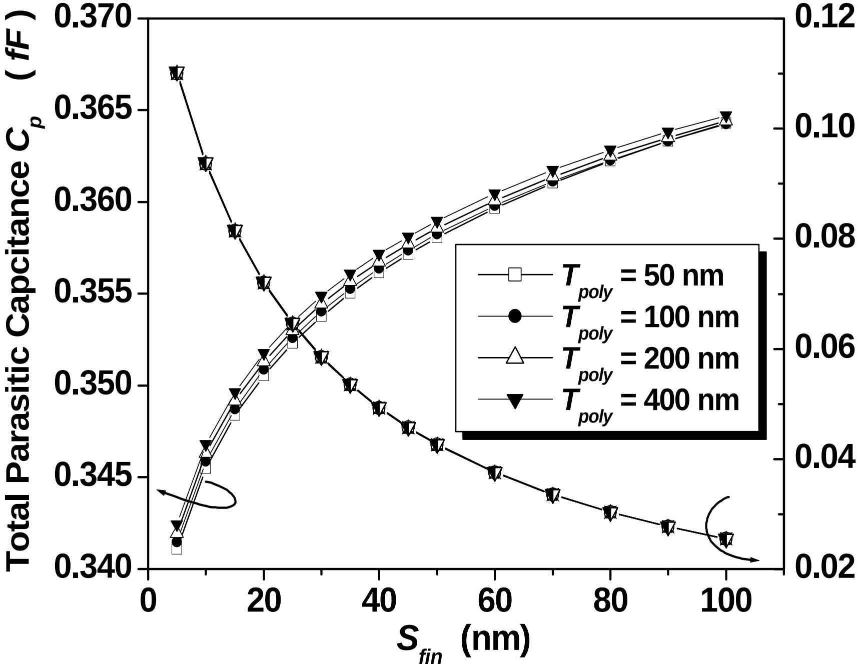
Three dimensional diagram of a two-fin double-gate MOSFET

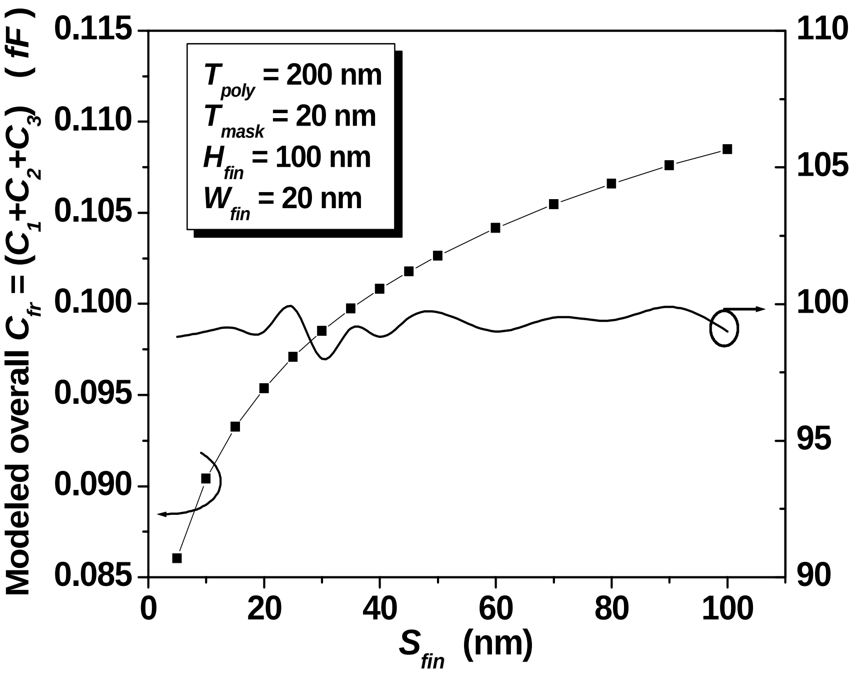


The top view of the 2-fin double-gate MOSFET

Fringing Capacitance Model

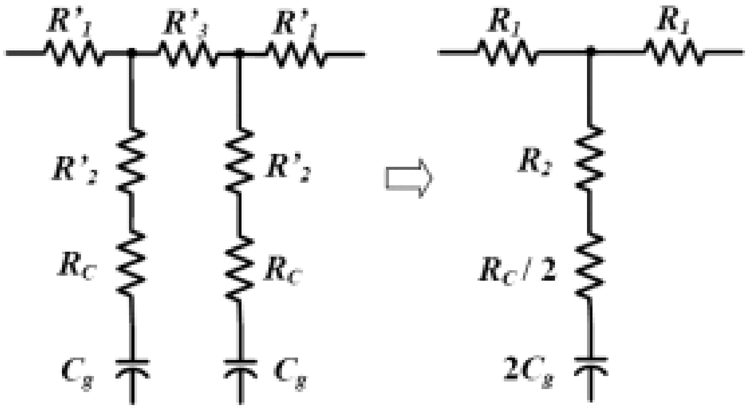
Comparison between model and 3-D numerical simulator





$$C_P = (C_1 + C_2 + C_2)$$

Gate Resistance Modeling



from π-network to *T*-network

$$R_1 = k_1\left(S_{fin} + 2T_{OX} + W_{fin}\right)/T_{poly}$$

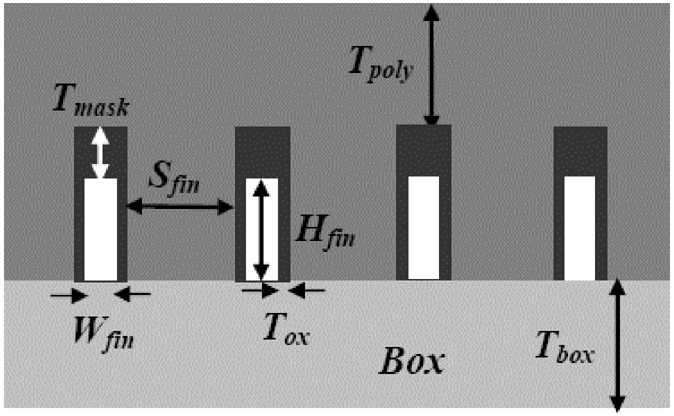
$$R_2 = k_2\left(T_{poly}/2 + T_{mask}\right)/S_{fin}$$

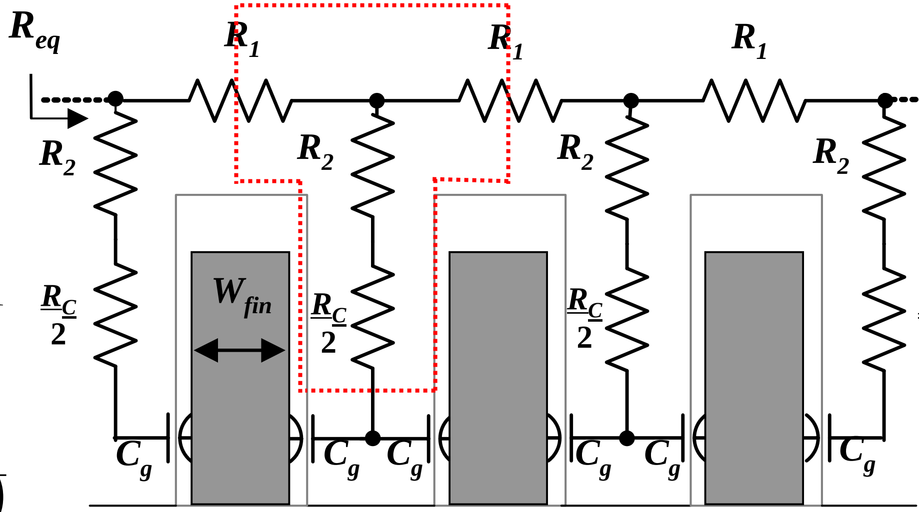
$$R_{eq,n} = \frac{(n-1)(R_2 + R_C/2)}{2n^2} + \frac{(n+1)(2n+1)R_1}{6n} + R_{eq,1}$$

$$C_{eq,n} = 2nC_g$$

⬇

$$S_{finopt} = \sqrt{\frac{3(n-1)T_{poly}\left(k_2 T_{poly}/2 + k_2 T_{mask} + \rho H_{fin}/3\right)}{n(n+1)(2n+1)k_1}}$$

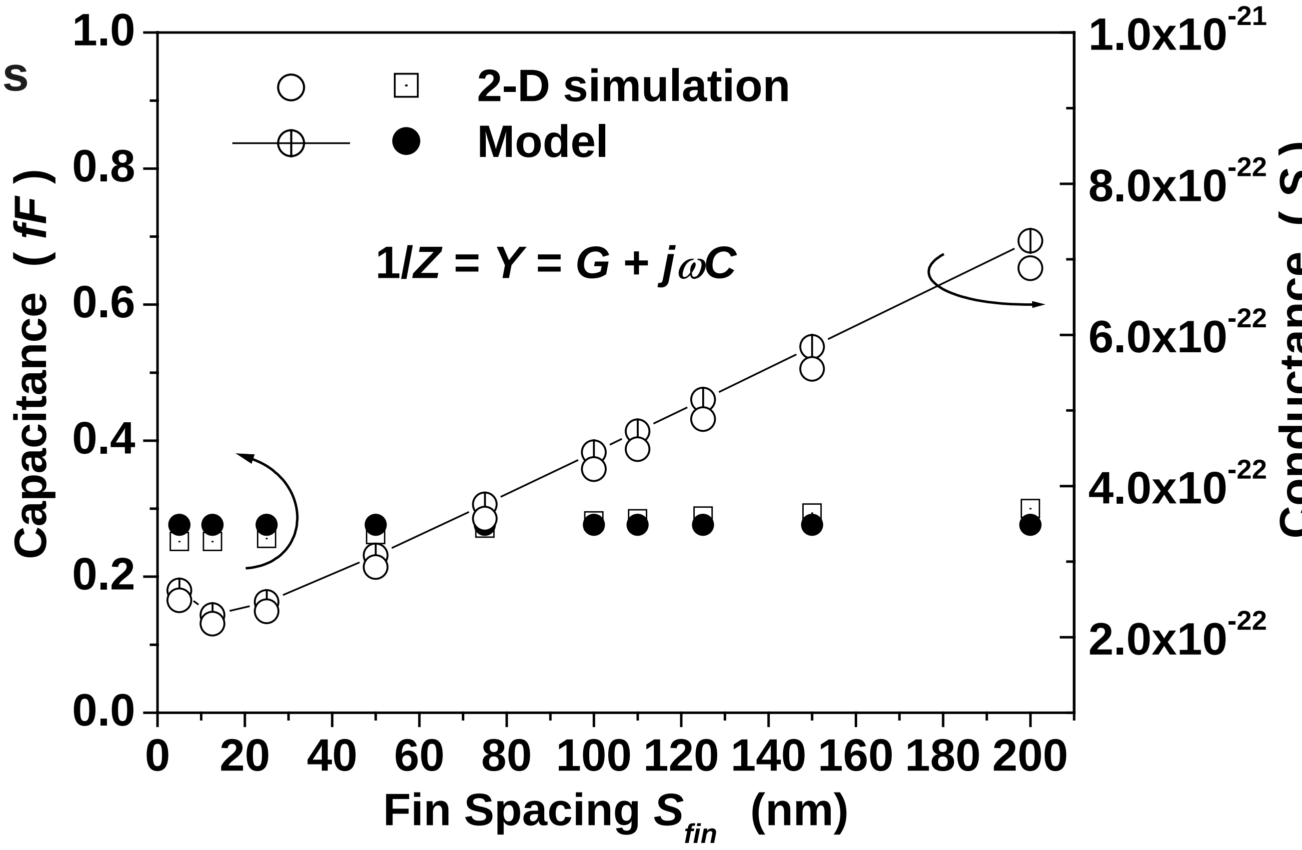




A RC network to model gate resistance

Gate Resistance Modeling

W_{fin} = 20 nm; H_{fin} = 80 nm
T_{OX} = 2 nm; L = 50 nm;
T_{mask} = 10 nm
The frequency (ω/2π) is 1000 Hz



$$Y = G + j\omega C = \frac{1}{R_{eq,n} + \frac{1}{j\omega C_{eq,n}}} \Rightarrow$$

$$\omega = 2\pi f \;; \quad C = C_{eq,n}$$

$$G = \omega^2 C_{eq,n}{}^2 R_{eq,n}$$

Summary

Project NDMI (Nano-Device Modeling Initiative), an international cooperative project, is aiming at:

- **Creation of a Platform for Compact Model Development Based on the Verilog-A Language**
- **Development of a Multi-Gate MOSFET Model with This Platform**

⇩

Final Output:

A Modular MG-MOSFET Model for Circuit Simulation Offering Continuous Enhancement Capability through the Plug-in of New Modules from Different Contributors