An Accurate and Versatile ED- and LD-MOS Model for High-Voltage CMOS IC SPICE Simulation

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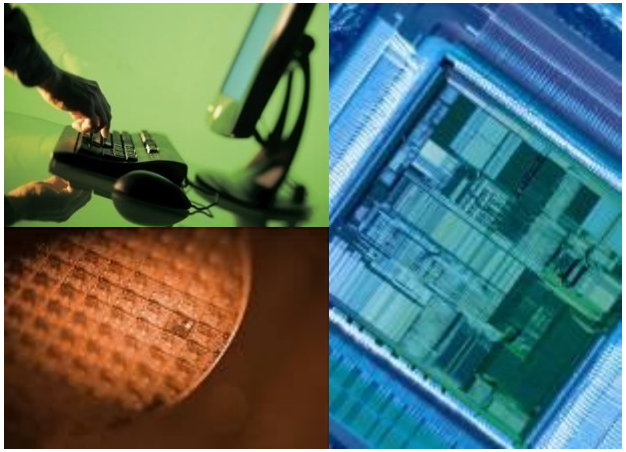

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Outline

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- Self Heating
- Impact Ionization in the Drift Region
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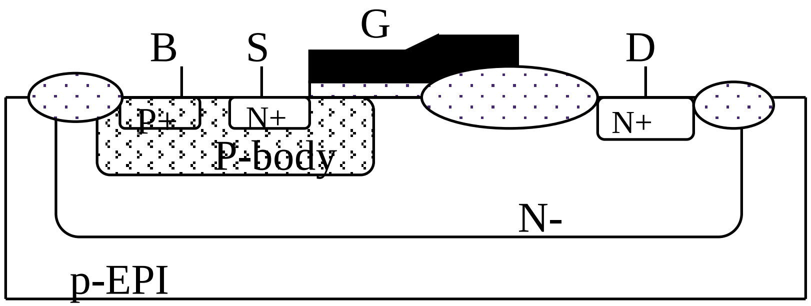
High Voltage MOSFET Modeling: Challenges

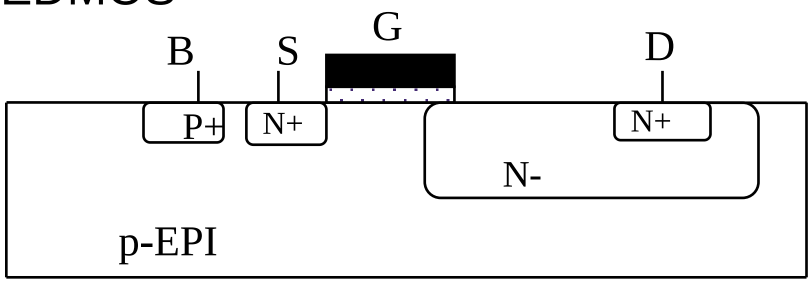
- **Large class of significantly different devices.**
  - **Integrated, low-medium power devices.**
  - **Discrete, high power devices.**
- **Many different device structures in the same class.**
- **Wide range of oxide thicknesses and biases.**
- **High voltage and self heating resulting in more circuit simulation convergence problems than in the case of low-voltage CMOS.**

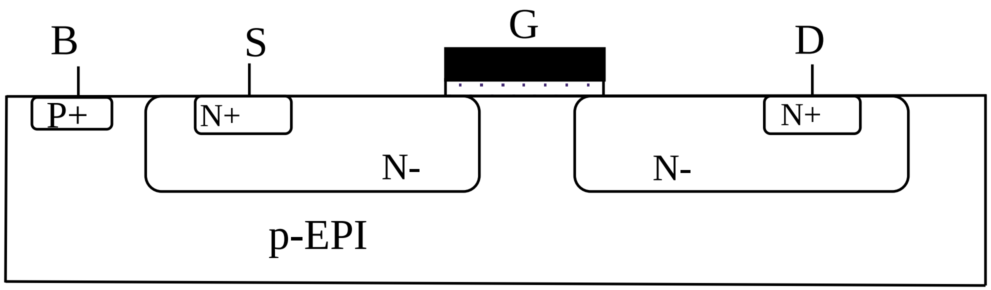
LDMOS and EDMOS

LDMOS

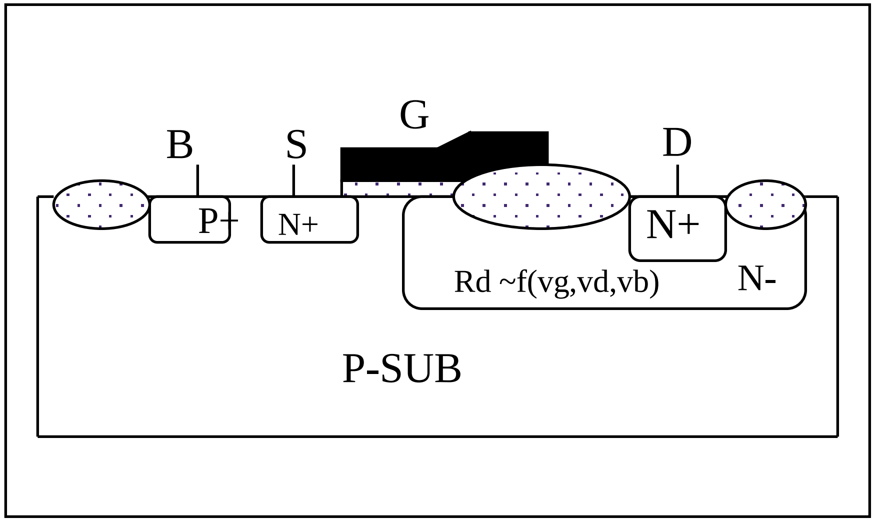


EDMOS

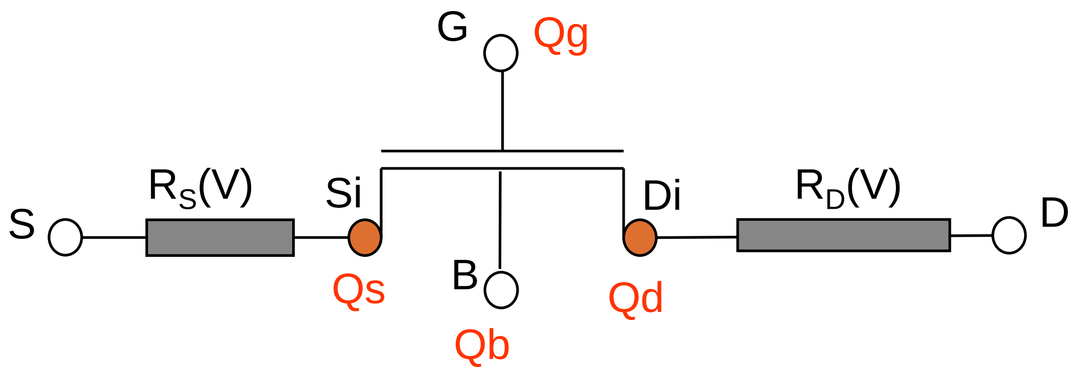




Conceptual Equivalent Structure

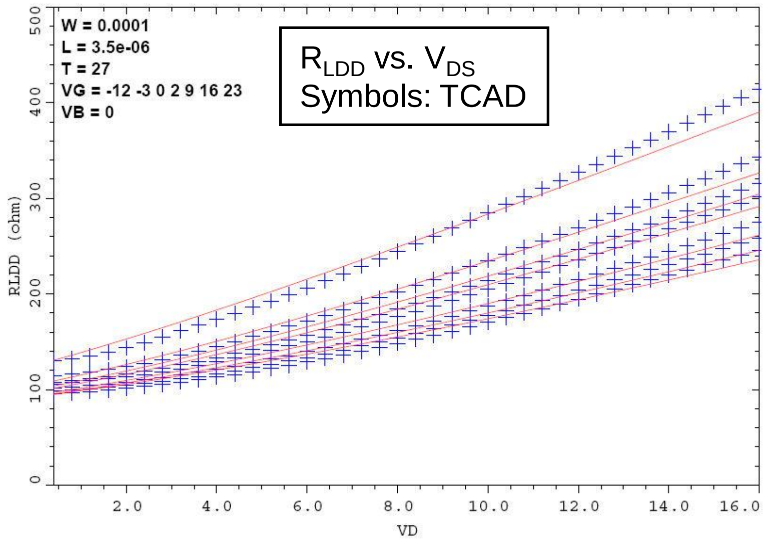


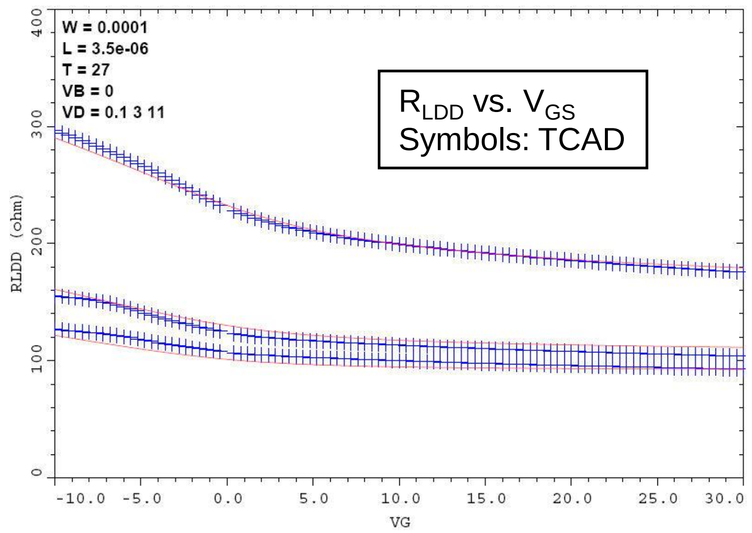
Model Topology

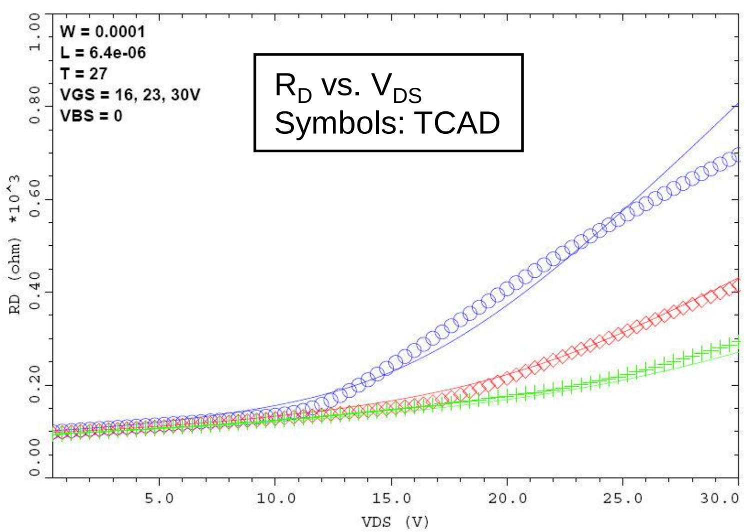


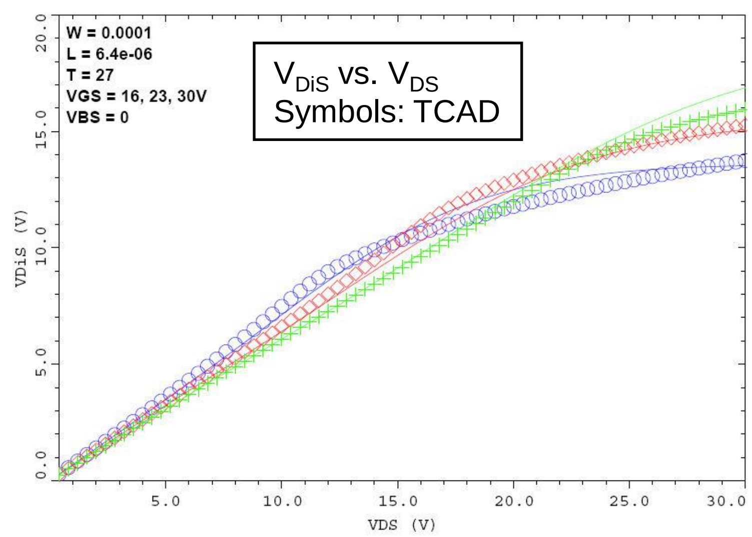
- **BSIM4-based:**
  - **Better voltage, geometry and temperature scaling.**
  - **Technology readiness for more advanced HV CMOS processes.**
  - **Strong capability for high-speed analog and RF power circuit simulation.**

Model Verification: TCAD





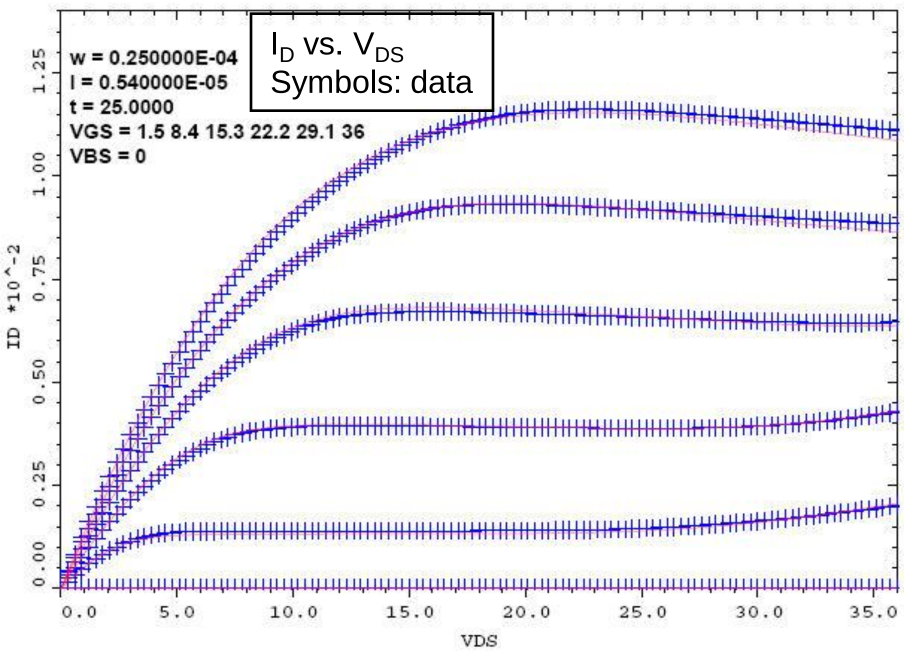


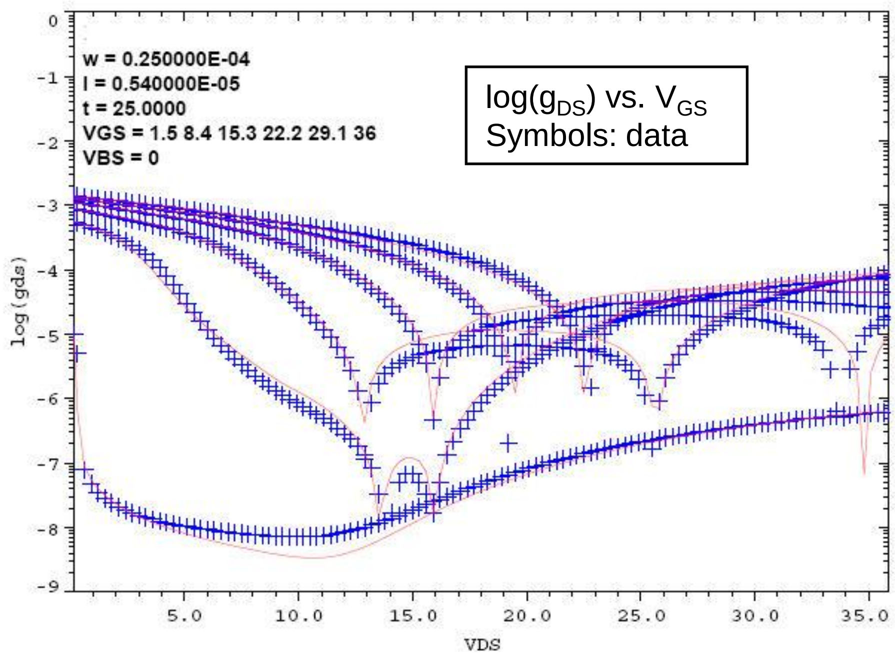


Predictable Success

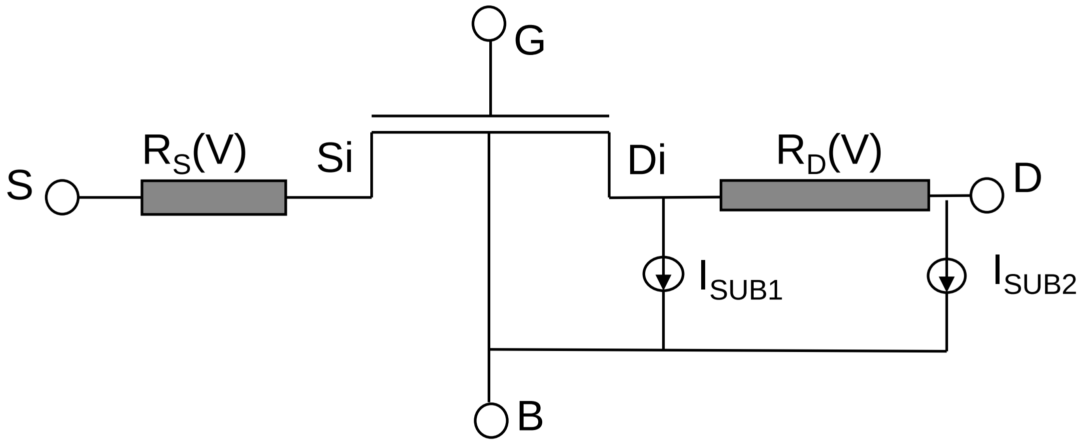
Self Heating

- **Scalable thermal network.**
- **Temperature-dependent R_{TH}.**

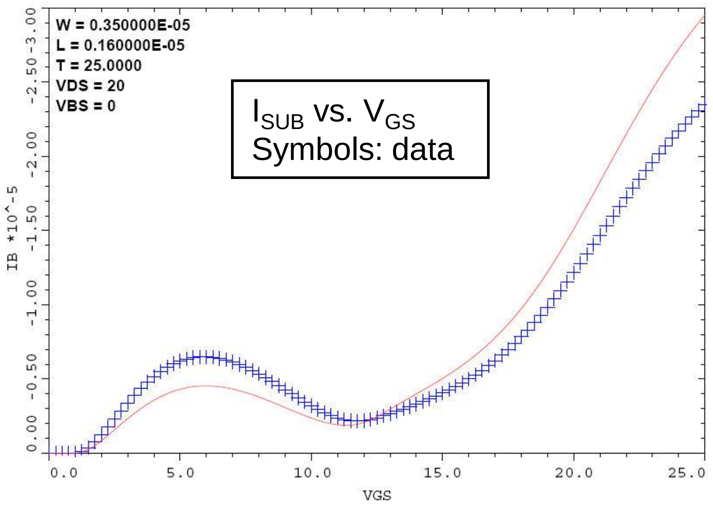


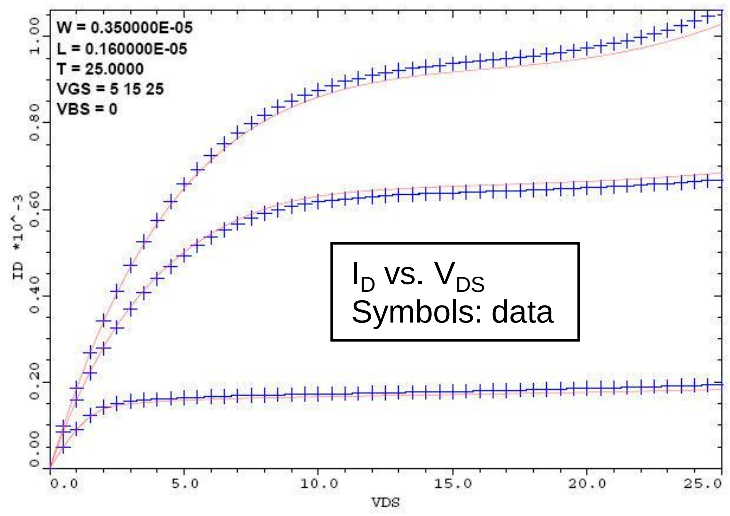


Impact Ionization in the Drift Region.

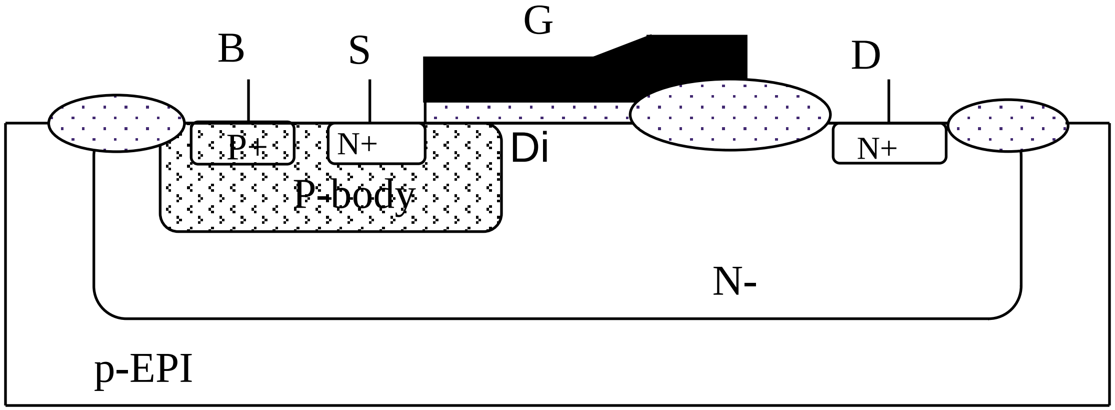


$$I_{SUB1} = f(V_{DiSi}) \cdot I_{DiSi} \qquad I_{SUB2} = f(V_{DDi}) \cdot I_{DDi}$$





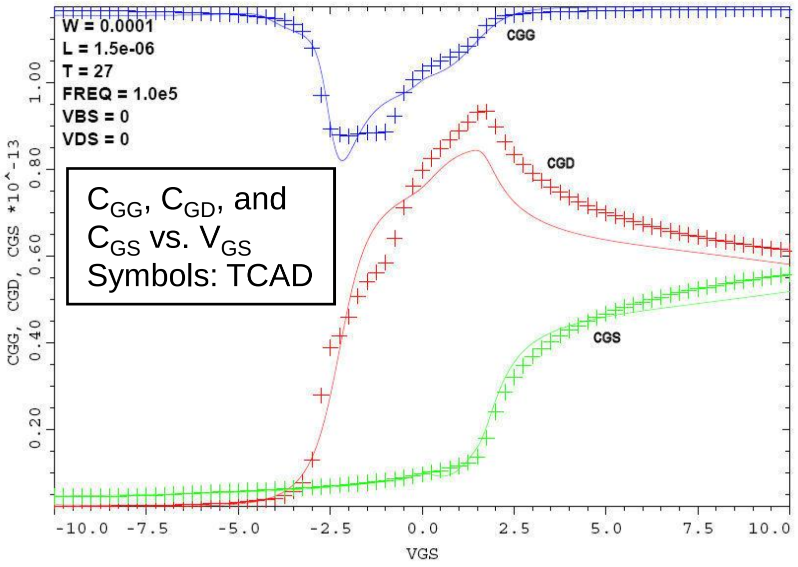
LDMOS-specific C-V Model



$$Q_{gtot} = Q_g + Q_{gx}$$
$$Q_{btot} = Q_b + Q_{bx}$$
$$Q_{dtot} = Q_d + Q_{dx}$$
$$Q_{stot} = Q_s$$

$$Q_{gx} = -(Q_{LDDinv} + Q_{LDDacc})$$
$$Q_{bx} = Q_{LDDinv}$$
$$Q_{dx}^{*} = Q_{LDDacc}$$

* Note : Q_{dx} is at node Di



Synopsys Predictable Success

Additional Effects

- Symmetric/Asymmetric geometries, leakage currents, and zero-bias capacitance densities for S/D-B junctions.
- Junction leakage due to carrier recombination and generation, various tunneling mechanisms, junction breakdown.
- Second-order temperature coefficients.
- Reverse mode-specific parameters.

Parameter Extraction

- **Multiple geometries, multiple temperatures.**
- **For asymmetric devices:**
  - **Reverse mode data, if available.**
  - **For EDMOS: characterize the symmetric device first, if available. Then, use the drain resistance parameters with the asymmetric device.**
- **Optimization based sequence:**
  - **Linear region parameters + some of the resistance parameters.**
  - **Most temperature coefficients (except the ones of VSAT).**
  - **Saturation region parameters: include all temperatures, self-heating parameters and VSAT temperature coefficients.**
  - **Capacitance parameters (for LDMOS: include C-V and I-V together and refine resistances and other parameters).**

Conclusions

- **Compact High Voltage MOSFET model, applicable to both LD- and ED-MOSFET devices.**
- **Consistently demonstrated very good accuracy and scalability over bias, geometry and temperature.**
- **No need for binning or macro-modeling.**
- **This model (Level=66) has been used in production by leading foundries and design houses.**