



Impact of Gate Induced Drain Leakage and Impact Ionization Currents on Hysteresis Modeling of PD SOI Circuits

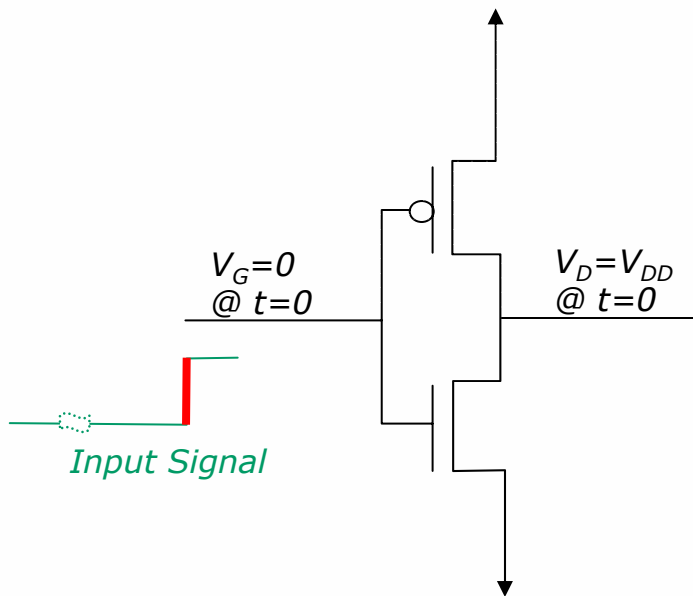
Qiang Chen, Jung-Suk Goo, Sushant Suryagandh,
Judy X. An, Ciby Thuruthiyil, and Ali B. Icel

May 23, 2007

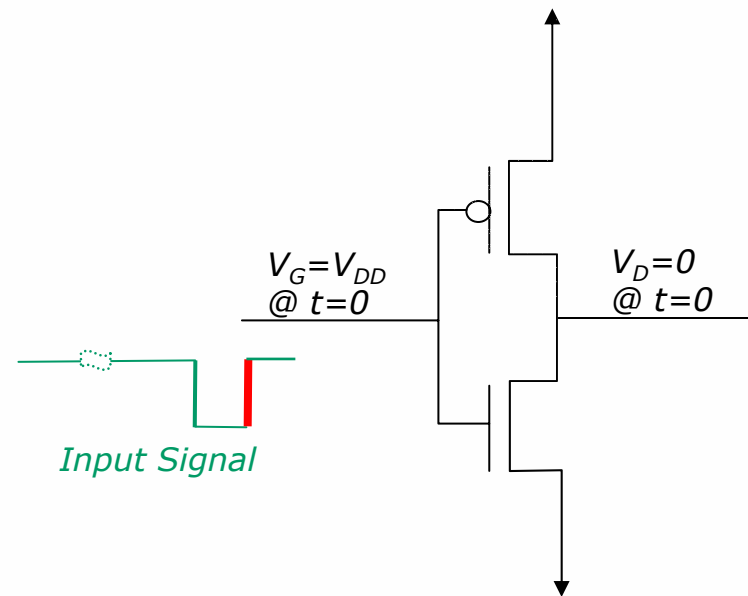
Outline

- **Hysteresis of Partially Depleted Floating-Body SOI Circuits**
- **Roles of GIDL and Impact Ionization Currents**
- **Silicon Data Analysis**
- **Compact Modeling Experiment**
- **Conclusions**

1st Switch, 2nd Switch, and Hysteresis



1st Switch (NFET Pull-down)



2nd Switch (NFET Pull-down)

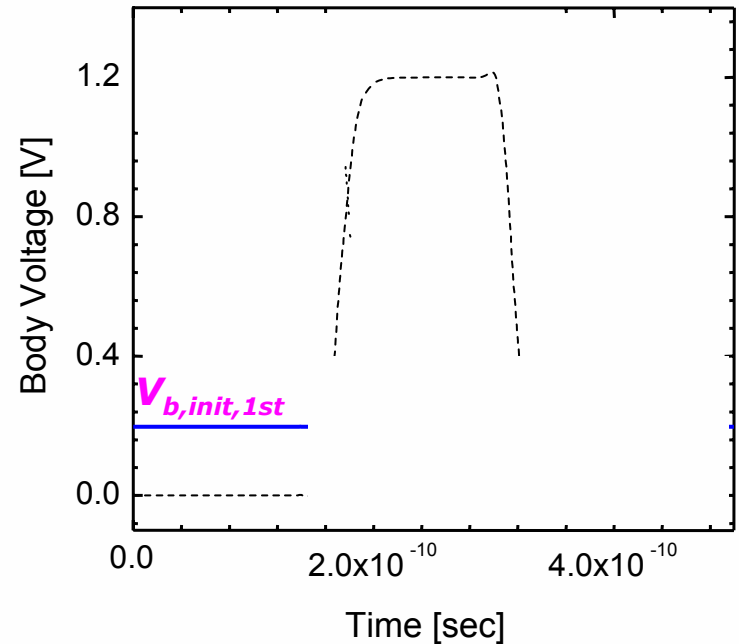
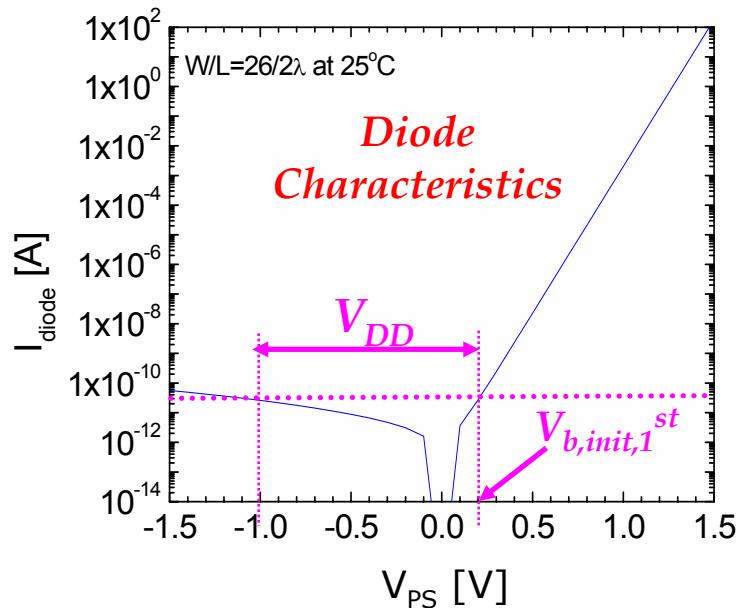
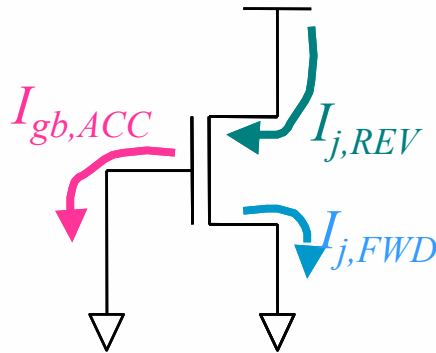
- Hysteresis defined as percentage difference of switch delays (FETs) or propagation delays (logic gates)

$$H = \frac{t_{PD}^{1st} - t_{PD}^{2nd}}{t_{PD}^{2nd}} * 100 \text{ [%]}$$

- Root cause: floating body potential

- ex., V_{BODY} increases $\rightarrow V_T$ decreases \rightarrow drive current increases \rightarrow delay decreases

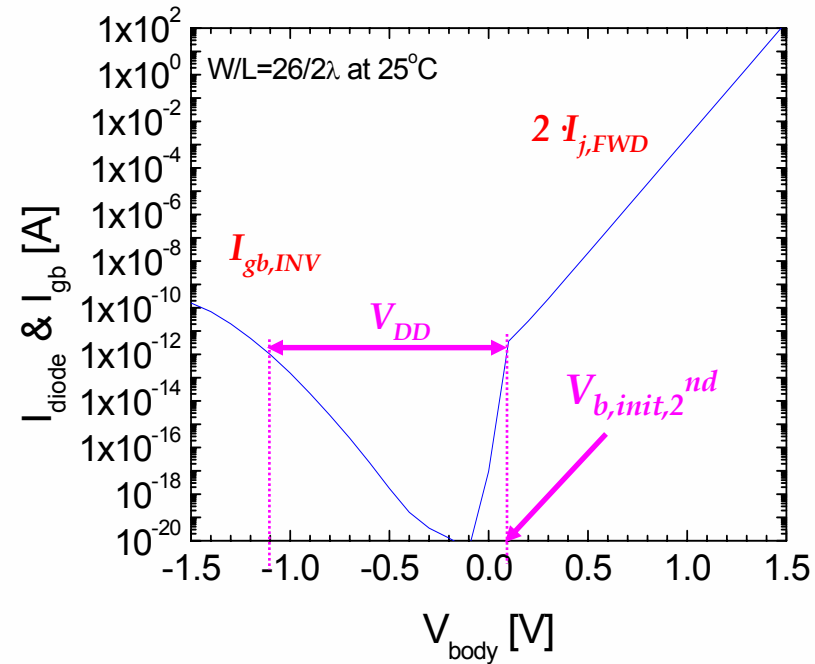
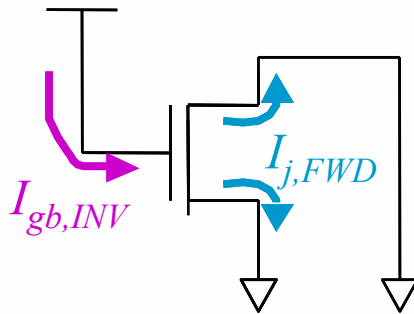
Pre-1st Switch V_{BODY}



V_{BODY} Evolution

J.-S. Goo, et al., "History-effect-conscious SPICE model extraction for PD-SOI technology", *IEEE SOI Conf.*, Oct. 2004, pp. 156-158

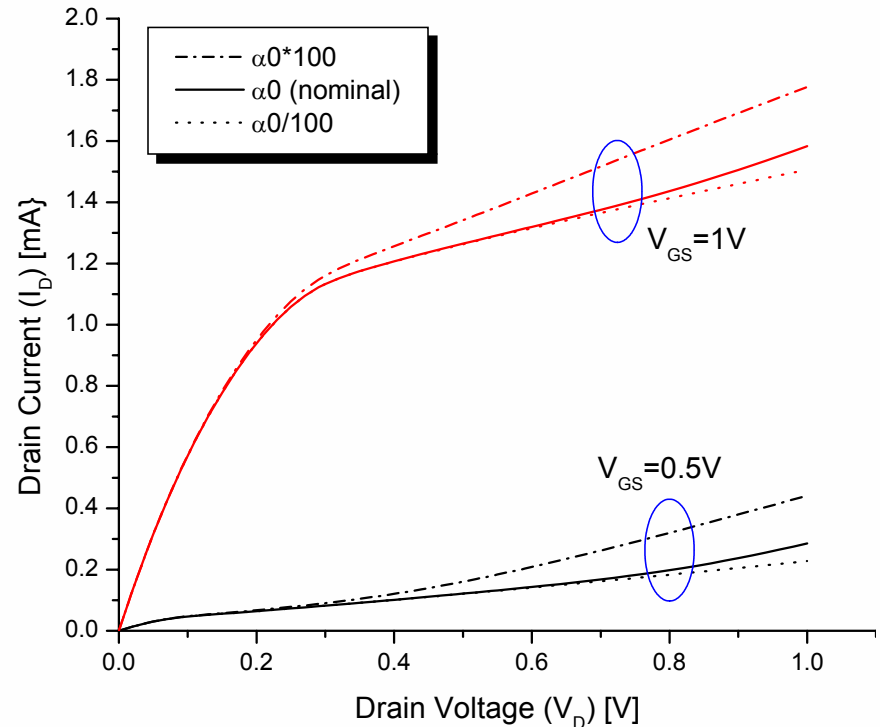
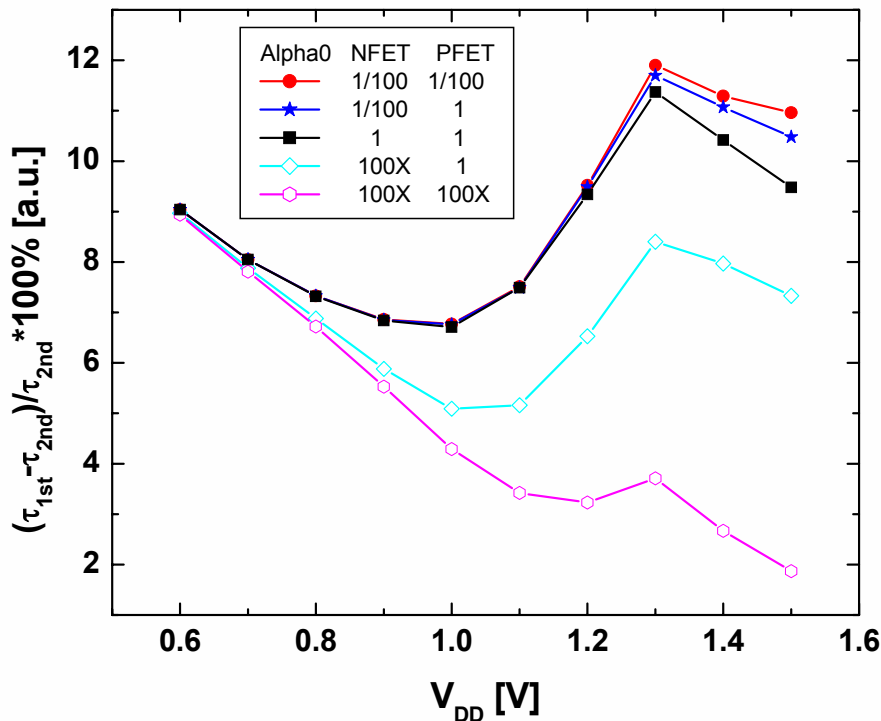
Pre-2nd Switch V_{BODY}



- $V_{b,int,2^{nd}}$ will be changed by gate/drain coupling prior to the 2nd switch to determine its delay

Observed Effect of Impact Ionization Current through Simulation

$$I_{ii} = \alpha_0 \left(I_{ds, MOSFET} + F_{bji} I_c \right) \exp \left(\frac{V_{diff}}{\beta_2 + \beta_1 V_{diff} + \beta_0 V_{diff}^2} \right) *$$



•How to understand the effect?

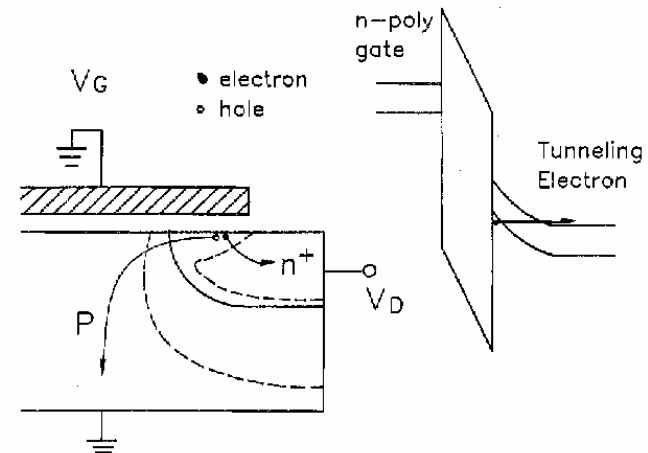
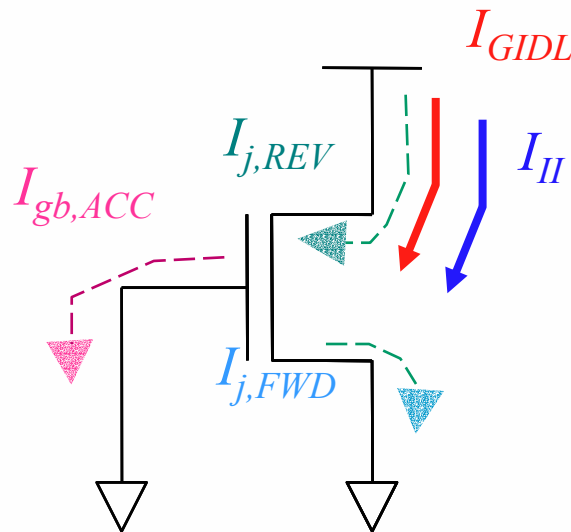
*BSIM PD/SOI manual, University of California at Berkeley, <http://www-device.eecs.berkeley.edu/~bsimsoi/get.html>

Outline

- Hysteresis of PD FB SOI Circuits
- Roles of GIDL and Impact Ionization Currents**
- Silicon Data Analysis
- Compact Modeling Experiment
- Conclusions

Revisit pre-1st Switch V_{BODY}

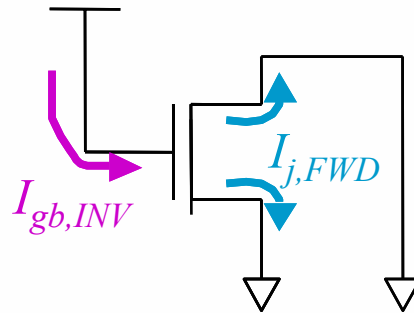
- Two additional parasitic currents may exist at zero V_{GS}
 - Gate induced drain current*
 - Impact ionization current: resulting from OFF-state channel leakage current
- They may contribute to V_{BODY} depending on their strength w.r.t. the reverse diode current, $I_{j,\text{REV}}$



*J. Chen, et al. "Subbreakdown drain leakage current in MOSFET," *IEEE EDL*, no.11, pp. 515-517, 1987

Revisit pre-2nd Switch V_{BODY}

- Previous analysis remains complete
 - GIDL and II currents have no effect on pre-2nd switch V_{BODY}



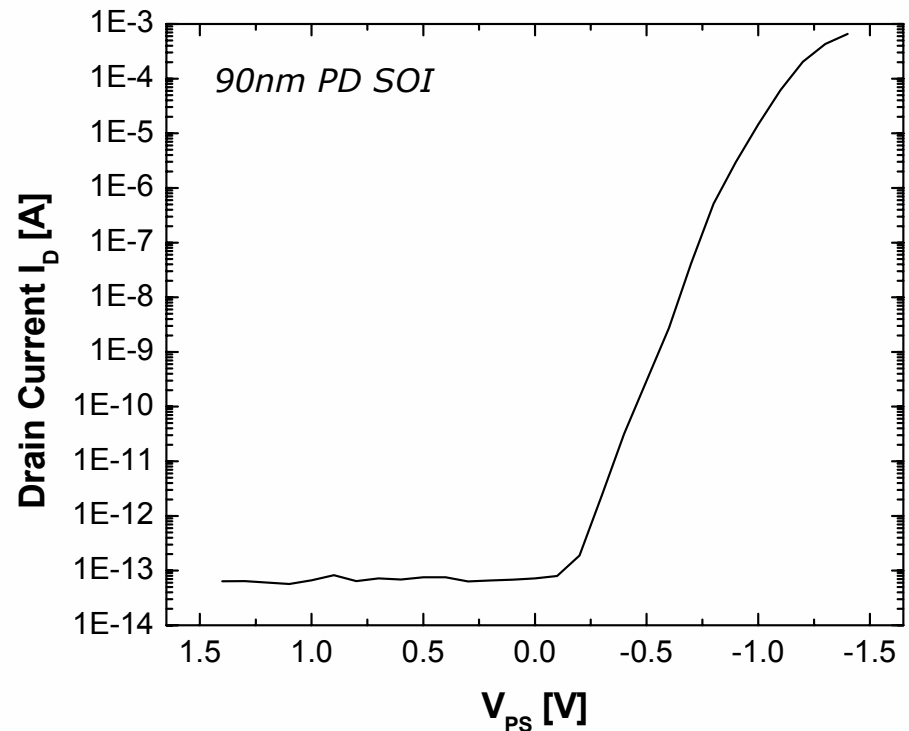
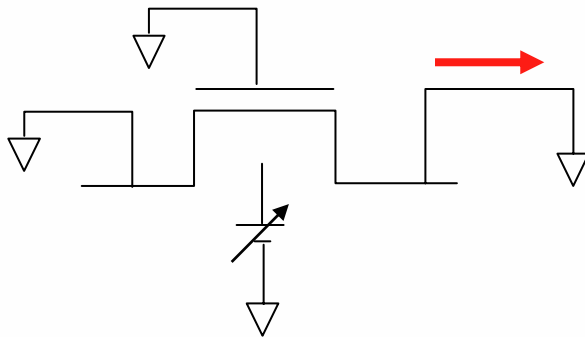
- Overall, hysteresis of PD SOI circuits *may* be affected by GIDL and II currents, specifically at zero V_{GS}

Outline

- Hysteresis of PD FB SOI Circuits
- Roles of GIDL and Impact Ionization Currents
- Silicon Data Analysis**
- Compact Modeling Experiment
- Conclusions

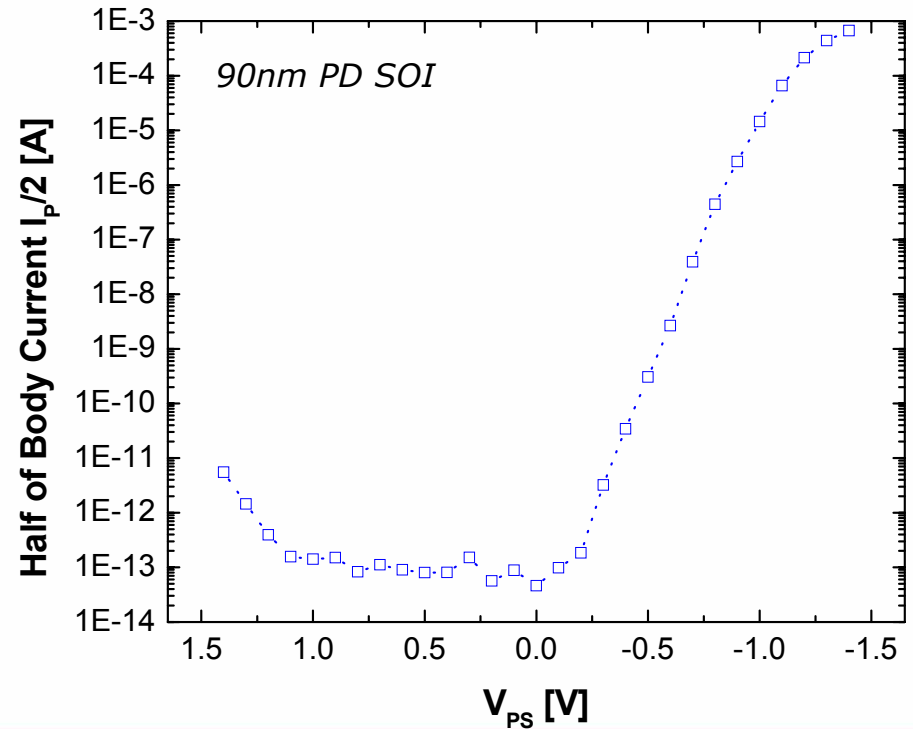
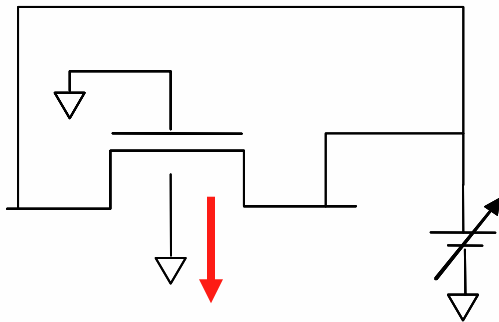
Junction Current Measurement

- Parasitic currents are characterized by using tied-body PD MOSFETs
- When the body is modulated, the substrate (i.e., body) current consists of junction currents and gate-to-body tunneling current
- Drain/source current represents pure junction current



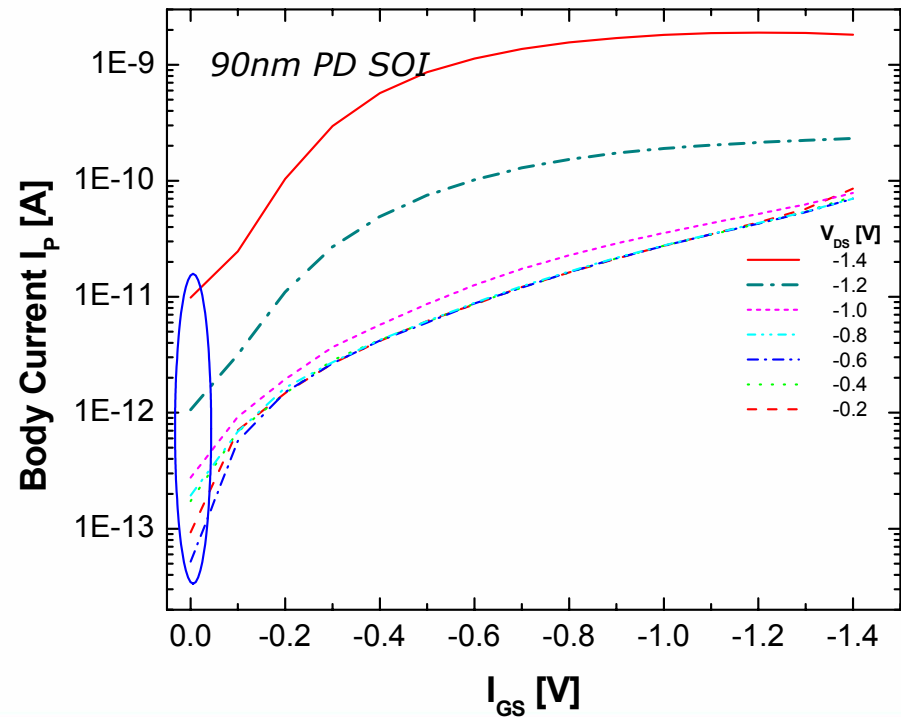
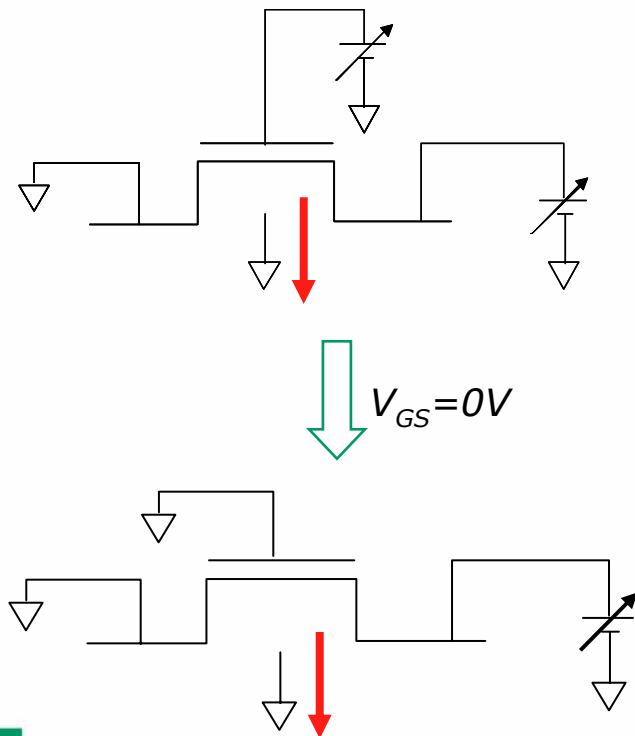
GIDL + Junction Currents

- The drain/source is modulated
- The substrate (i.e., body) current consists of junction currents and GIDL current



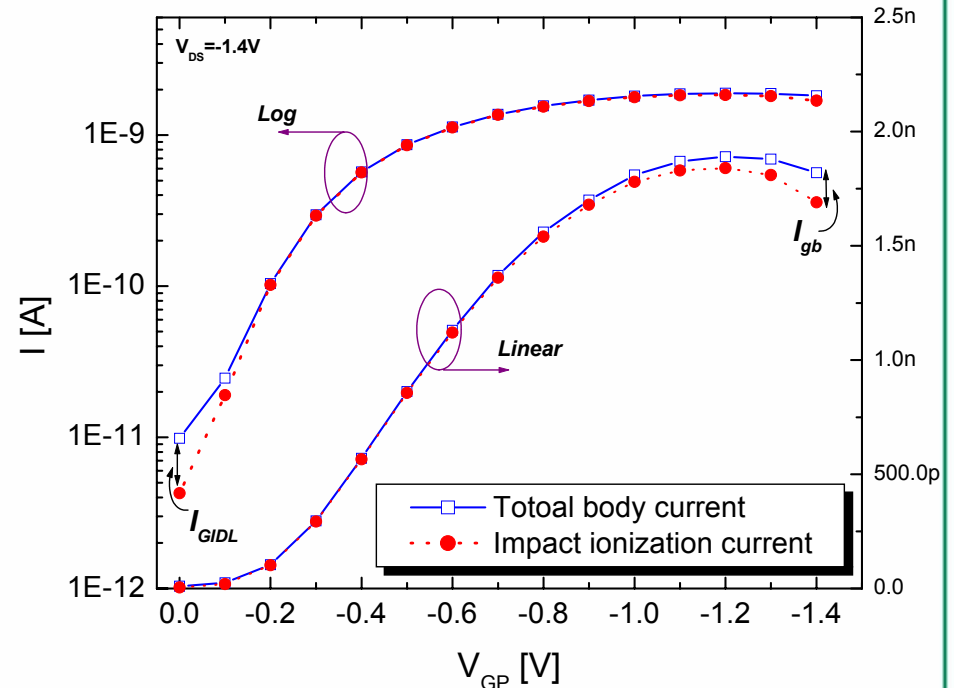
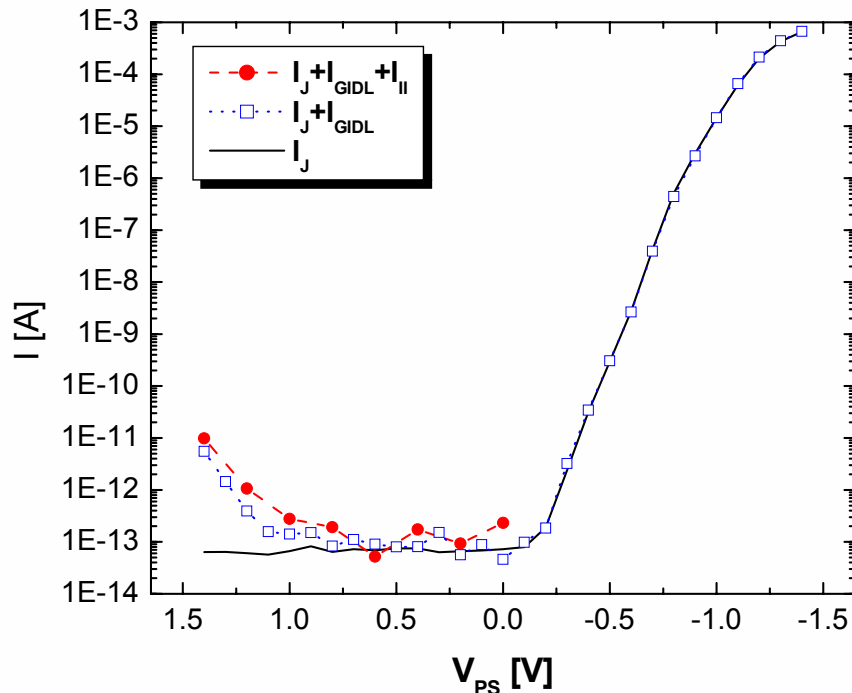
Substrate Current Measurement

- Standard substrate current measurement
- The substrate current at $V_{GS}=0V$ (circled) consists of junction current, GIDL, and impact ionization current



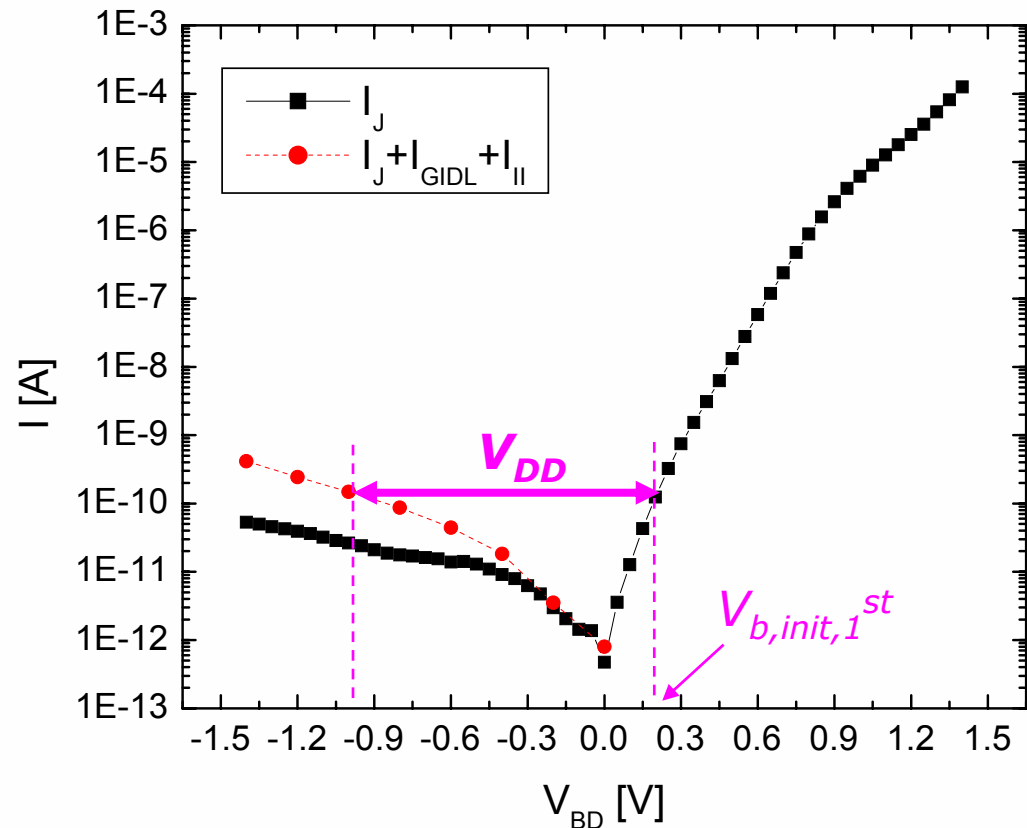
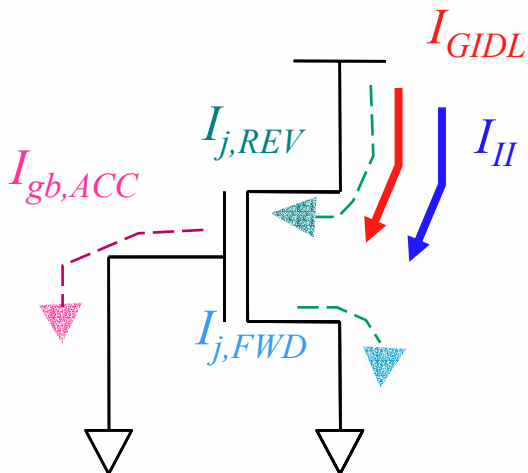
Put All Pieces Together..

- GIDL and II currents are comparable to each other, both significantly larger than the reverse diode current



Similar Data in 65nm PD SOI

- GIDL and impact ionization currents indeed may affect pre-1st switch V_{BODY} , and consequently hysteresis in advanced SOI technologies



Outline

- Hysteresis of PD FB SOI Circuits
- Roles of GIDL and Impact Ionization Currents
- Silicon Data Analysis
- Compact Modeling Experiment**
- Conclusions

Three PMOS Model Cards under Test

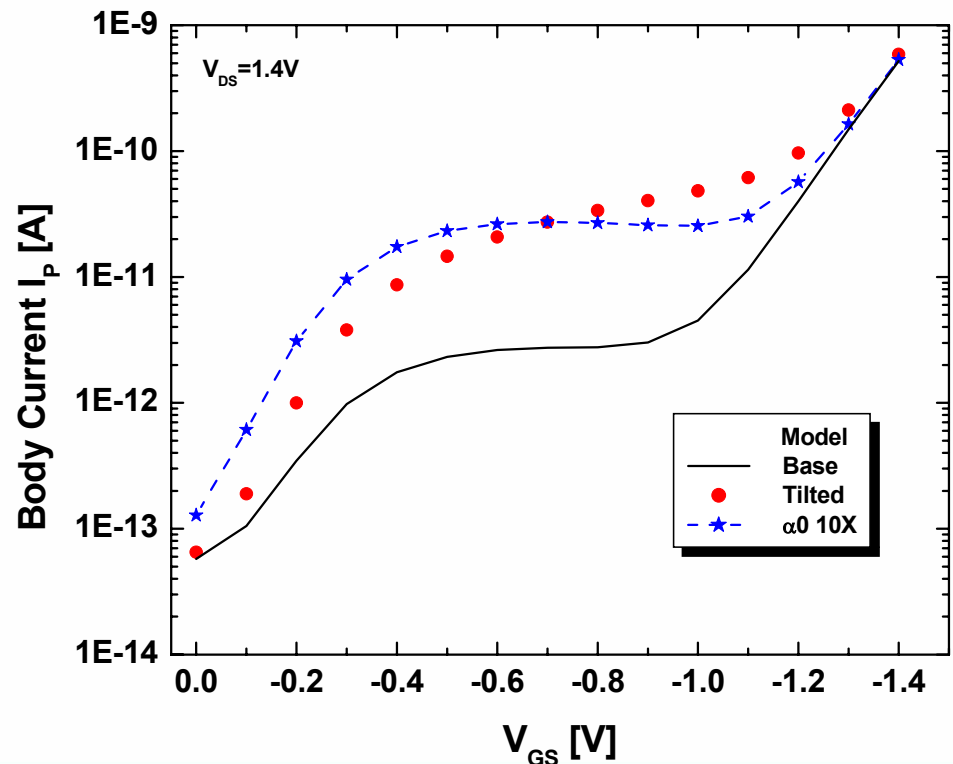
- Three model cards are ~identical except for the substrate current
- 'α₀ 10x' model derived from the base model by increasing α₀ by 10
- 'Tilted' model derived from the base model by changing α₀, v_{dsat}i₀, s_{ii}0

$$I_{tt} = \alpha_0 I_{ds,MOSFET} + F_{bjtt} I_c \exp\left(\frac{V_{diff}}{\beta_2 + \beta_1 V_{diff} + \beta_0 V_{diff}^2}\right)$$

$$V_{diff} = V_{ds} - V_{dsat}$$

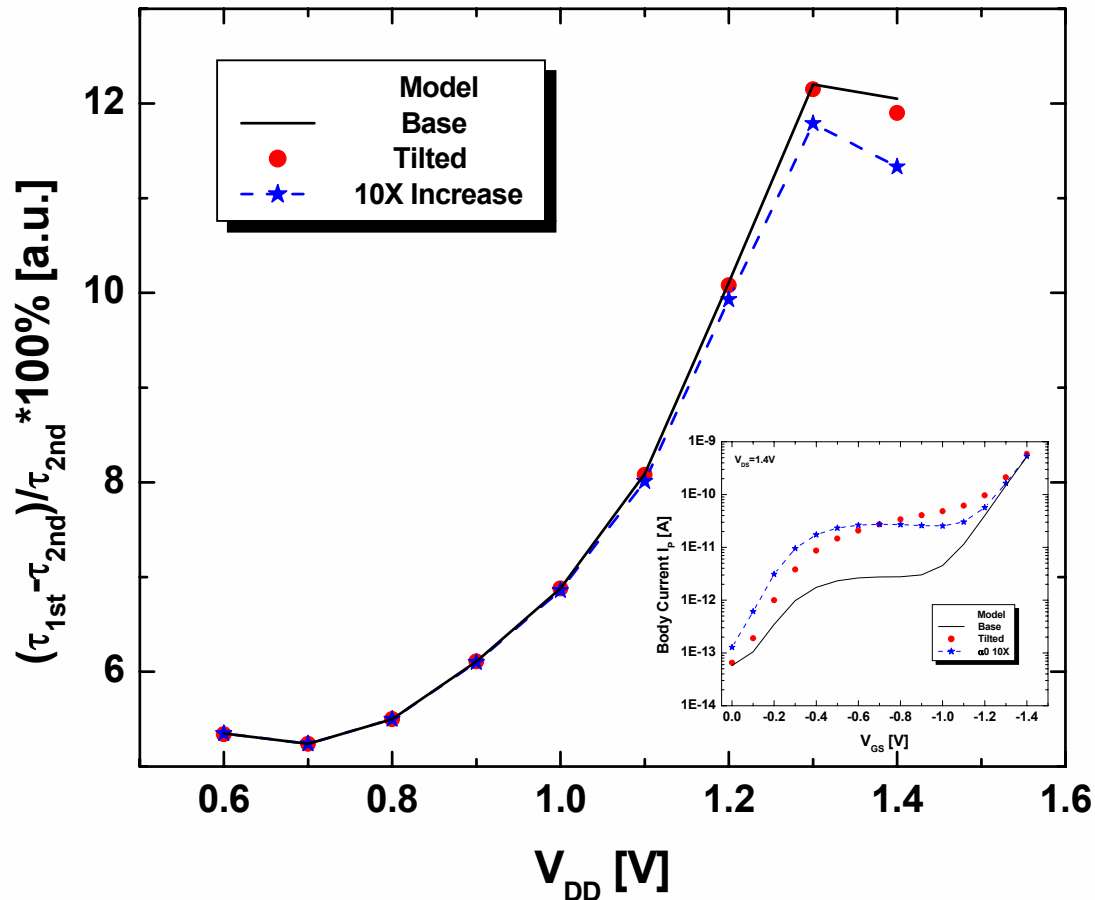
$$V_{dsat} = V_{gs}Step + \left[V_{dsat}0 \left(1 + T_{tt} \left(\frac{T}{T_{nom}} - 1 \right) \right) - \frac{L_{tt}}{L_{eff}} \right]$$

$$V_{gs}Step = \left(\frac{E_{sat} L_{eff}}{1 + E_{sat} L_{eff}} \right) \left(\frac{1}{1 + S_{in} V_{gsteff}} + S_{ii2} \left(\frac{S_{ii0} V_{gst}}{1 + S_{ii0} V_{ds}} \right) \right)$$



Hysteresis Simulations

- Simulation results confirm that GIDL and II currents at zero V_{GS} only matter for hysteresis



Outline

- Hysteresis of PD FB SOI Circuits
- Roles of GIDL and Impact Ionization Currents
- Silicon Data Analysis
- Compact Modeling Experiment
- Conclusions**

Conclusions

- Re-examined parasitic currents in PD SOI MOSFETs and their impact on hysteresis, revealing that GIDL and impact ionization currents at zero V_{GS} may contribute to the pre-1st switch body voltage, and consequently hysteresis.
- Analyzed silicon data of parasitic currents in 90nm and 65nm PD SOI technologies by using various measurement schemes. The results indicate that GIDL and II currents at zero V_{GS} are comparable to each other, both significantly larger than the reverse diode current.
- A modeling experiment confirms that in the standard substrate current measurement data, only those at zero V_{GS} matter for hysteresis modeling.
- As scaling continues and threshold voltage reduces, GIDL and II currents at zero V_{GS} need to be closely monitored and well modeled for hysteresis prediction.

Trademark Attribution

AMD, the AMD Arrow logo and combinations thereof are trademarks of Advanced Micro Devices, Inc. in the United States and/or other jurisdictions. Other names used in this presentation are for identification purposes only and may be trademarks of their respective owners.

©2007 Advanced Micro Devices, Inc. All rights reserved.