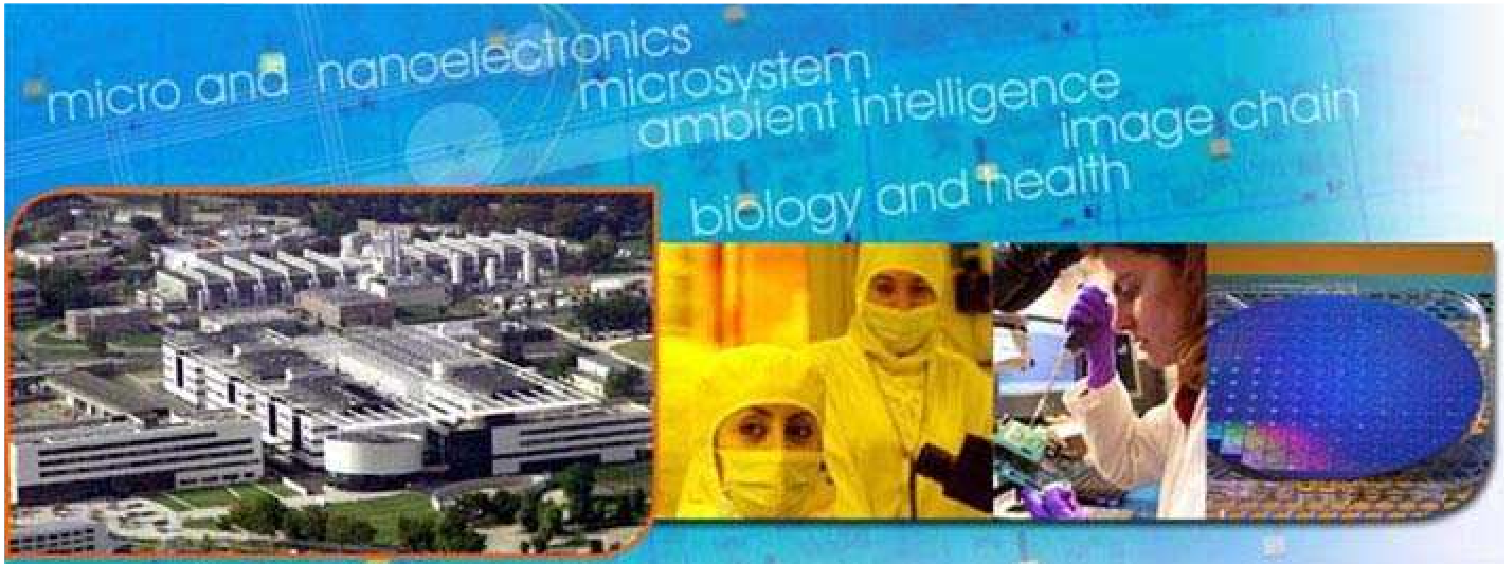

2007

Explicit Short Channel Compact Model of Independent Double Gate MOSFET

M. Reyboz, O. Rozeau, T. Poiroux,

P. Martin , M. Cavelier and J. Jomaah

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OUTLINE

I Introduction

II Physical & Mathematical Difficulties of Compact Modeling of IDG MOSFET

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V Conclusion & Prospects

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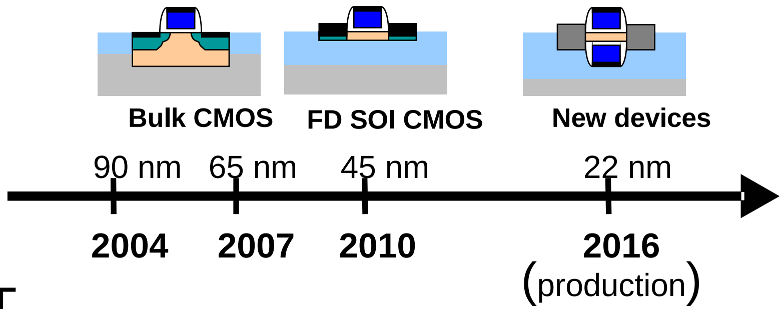
INTRODUCTION

General Context

NEW DEVICES

classical CMOS technologies **+**
forecast of the ITRS Roadmap **=** ?
New devices appear: GAA, FinFET, SON & planar DG MOSFET



- ✓ **Excellent electrostatic control** thanks to a better coupling between gate & channel (mainly for SG MOS) ➡ better I_{on}/I_{off} ratio
- ✓ **Almost twice more** I_{on} current than a classical MOSFET with one gate
- ✓ **More flexibility** thanks the second gate which can be independently driven for an IDG MOSFET
- ✓ **Undoped film** ➡ no more doping fluctuation in the channel

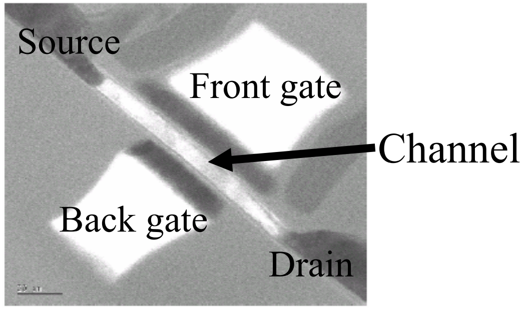
MODEL

To take advantage of this new device, designers need a model, particularly a compact model to design new circuits

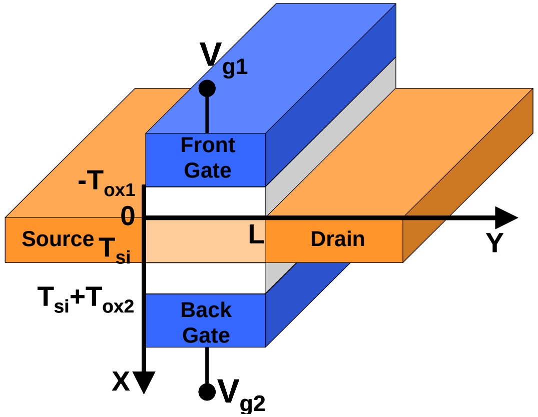
INTRODUCTION

Different Kinds of DG MOSFET

T_{si}: 10nm
T_{ox1} & T_{ox2}:1.2nm
L: 10nm to 1µm



IDG MOSFET
M.Vinet *et al*, SSDM 2004



ADG MOSFET:

- different gate oxide thicknesses
- and/or different gate functions

IDG MOSFET: gates are independently driven

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PHYSICAL & MATHEMATICAL DIFFICULTIES

Basic Equations of an IDG MOSFET

Drain current

$$I_{ds} = \mu \frac{W}{L} \int_{V_s}^{V_d} Q_{inv}\, d\phi_{imref}$$

Gauss theorem

$$Q_{inv} = \varepsilon_{si}(E_{s1} - E_{s2})$$

Boundary conditions

$$E_{s1} = \frac{c_{ox}}{\varepsilon_{si}}(V_{g1} - \psi_{s1})$$

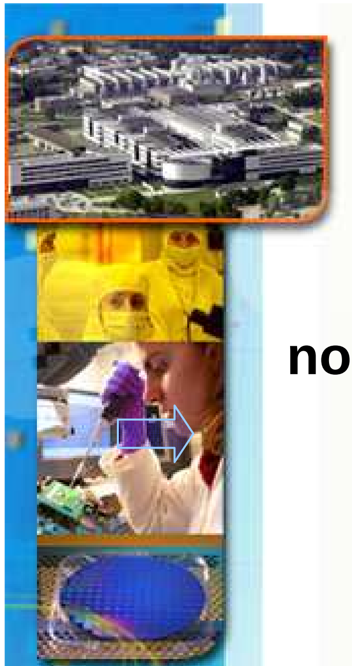
$$E_{s2} = -\frac{c_{ox}}{\varepsilon_{si}}(V_{g2} - \psi_{s2})$$

Poisson equation & its first integration

$$\frac{d^2\psi}{dx^2} = \frac{q.n}{\varepsilon_{si}}$$

$$E_{s1}^2 - E_{s2}^2 = \frac{2.q.u_t.n_i}{\varepsilon_{si}}\left[\exp\left(\frac{\psi_{s1} - \phi_{imref}}{u_t}\right) - \exp\left(\frac{\psi_{s2} - \phi_{imref}}{u_t}\right)\right]$$

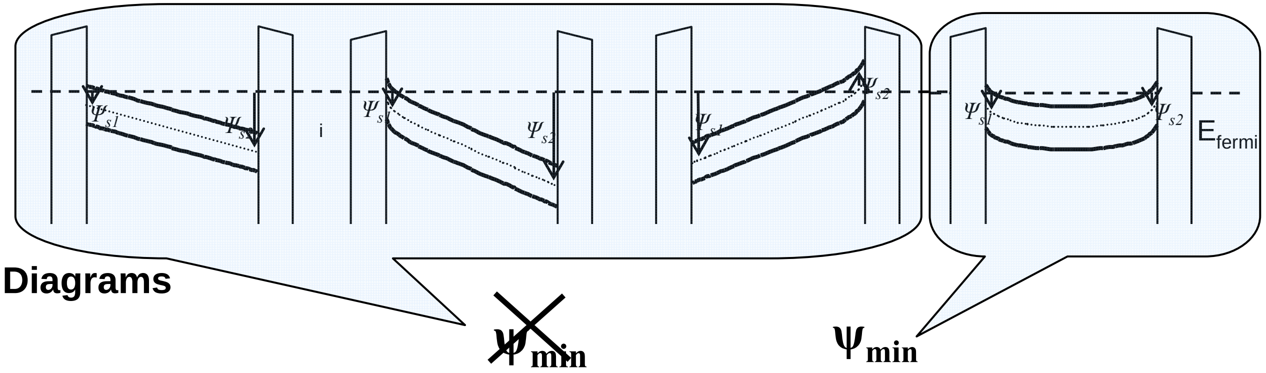
➡ **To physically derive I_{ds}, surface potentials ψ_{s1} & ψ_{s2} should be known**



PHYSICAL & MATHEMATICAL DIFFICULTIES

Mathematical Difficulties

ASYMETRICAL or INDEPENDENT GATE DEVICES
not always a minimum of potential in the silicon film: 2 CASES should be distinguished



Band Diagrams

First difficulty

Two cases should be defined

Second difficulty

There is no exact solution of ψ_{s1} & ψ_{s2}

Numerical resolution in the model code

4 unknown parameters: $\psi_{s1Source}$, $\psi_{s1Drain}$ & $\psi_{s2Source}$, $\psi_{s2Drain}$

To make physical assumptions

➡ Simplifications Poisson equation

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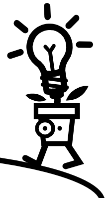
THRESHOLD VOLTAGE BASED COMPACT MODEL

Long Channel Model



PRINCIPLE

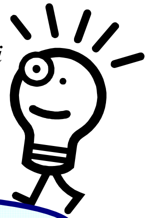
$$\boxed{Q_{inv} = Q_{inv1} + Q_{inv2}}$$

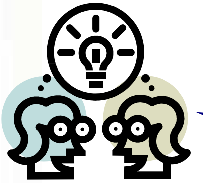
$$Q_{invi}^{WI}(x) = -q.N_i.u_t.\exp\left(\frac{V_{gi} - V_{thi} - n_i.\phi_{imref}}{n_i.u_t}\right)$$

i = 1 or 2

$$Q_{invi}^{SI}(x) = -C_{oxi}.\left(V_{gi} - V_{thi} - n_i.\phi_{imref}(x)\right)$$

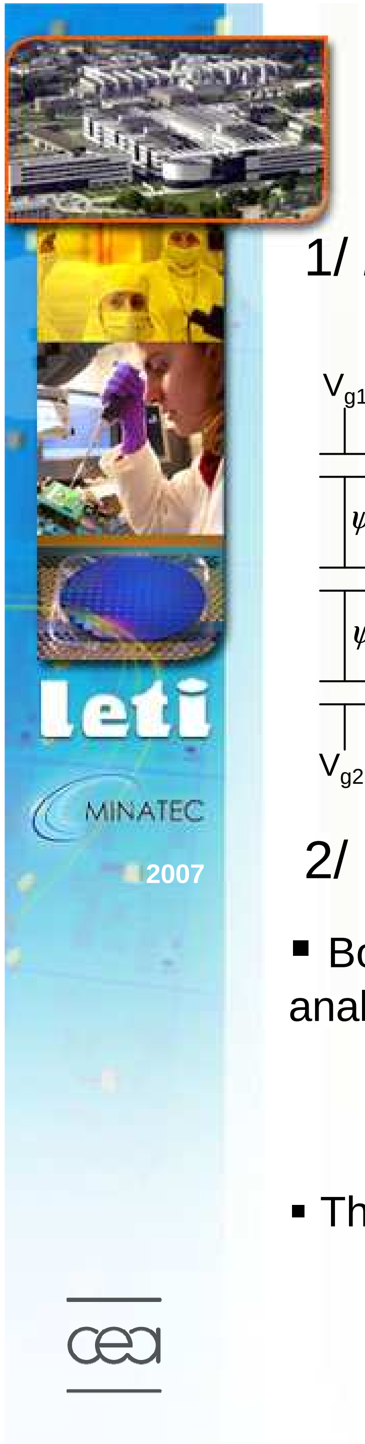
q is the electronic charge, N_i intrinsic concentration of carriers, u_t is the thermal voltage Φ_{imref} the quasi level of Fermi of electrons in the channel, V_{gi} are the front and the back voltages and C_{oxi} the front and the back gate oxides.





We know how to link the following equations

Now, n_i (coupling factor) and V_{thi} (threshold voltage) should be expressed analytically and explicitly

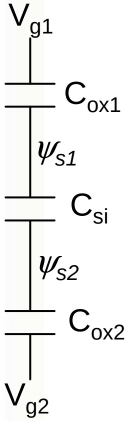


THRESHOLD VOLTAGE BASED COMPACT MODEL

Long Channel Model

1/ n_i expressions, the coupling factors

Physical assumption in weak inversion at both interfaces: Transverse electrical field is uniform because the channel is undoped



$$\psi_{s1} = \left(1 - \frac{C_{si} C_{ox2}}{C_{si} C_{ox1} + C_{ox1} C_{ox2} + C_{si} C_{ox2}}\right) V_{g1} + \frac{C_{si} C_{ox2}}{C_{si} C_{ox1} + C_{ox1} C_{ox2} + C_{si} C_{ox2}} V_{g2}$$

$$\Downarrow$$

$$\psi_{s1} = \frac{1}{n_1} V_{g1} + \frac{n_1 - 1}{n_1} V_{g2}$$

2/ V_{thi} expressions, the threshold voltages

- Both interfaces are in weak inversion, inversion charges Q_{inv1} & Q_{inv2} are analytically expressed as:

example

$$Q_{inv1} = -q.N_i \frac{T_{Si}}{2} u_t \exp\left(\frac{\psi_{S1} - \phi_{imref}}{u_t}\right) \frac{\tanh\left[\frac{C_{eq}}{C_{Si}} \frac{V_{g2} - V_{g1}}{2.u_t}\right]}{\frac{C_{eq}}{C_{Si}} \frac{V_{g2} - V_{g1}}{2.u_t}}$$

- These expressions are identified with:

$$Q_{invi}^{WI}(x) = -q.N_i.u_t.\exp\left(\frac{V_{gi} - V_{thi} - n_i.\phi_{imref}}{n_i.u_t}\right)$$

THRESHOLD VOLTAGE BASED COMPACT MODEL

Long Channel Model

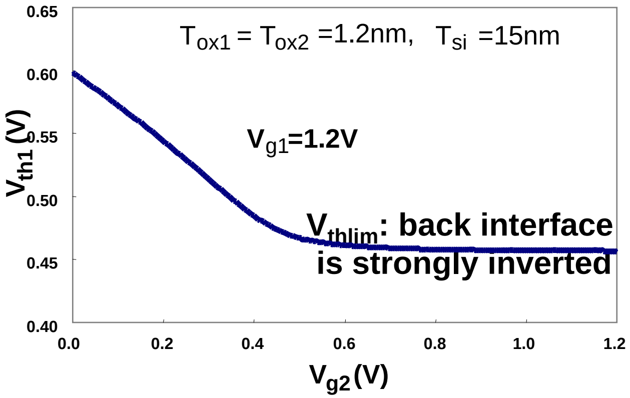
2/ V_{thi} expressions, the threshold voltages

$$V_{th1}=n_1u_t\ln\left[\frac{2n_1C_{ox1}u_t}{q.N_iT_{Si}}\right]-(n_1-1)V_{g2}-n_1u_t\ln\left(\frac{\tanh\left[\frac{C_{eq}}{C_{Si}}\frac{V_{g2}-V_{g1}}{2u_t}\right]}{\frac{C_{eq}}{C_{Si}}\frac{V_{g2}-V_{g1}}{2u_t}}\right)$$

$$V_{th2}=n_2u_t\ln\left[\frac{2n_2C_{ox2}u_t}{q.N_iT_{Si}}\right]-(n_2-1)V_{g1}-n_2u_t\ln\left(\frac{\tanh\left[\frac{C_{eq}}{C_{Si}}\frac{V_{g2}-V_{g1}}{2u_t}\right]}{\frac{C_{eq}}{C_{Si}}\frac{V_{g2}-V_{g1}}{2u_t}}\right)$$

3/ Strong inversion description

- We enlarge when both interfaces are at threshold ➡ $V_{thi,lim}$ is defined



THRESHOLD VOLTAGE BASED COMPACT MODEL

Long Channel Model

3/ Strong inversion description

- We add a correction factor to model the non total screening of the channel by the inversion charge

ε_i represents the dependence of a strong inverted interface versus its gate voltage

$$Q_{invi}^{SI}(x) = -C_{oxi}\left(V_{gi} - V_{thi} - n_i.\phi_{imref}(x)\right)\left(1-\varepsilon_i(x)\right)$$

Q_{invi} expressions, boundary conditions & the fact that the weak inversion charge can be neglected, we get an explicit ε_i

4/ Drain current expressions

$$I_{dsi} = -\frac{W}{L}\mu\int_0^{V_{ds}} Q_{invi}(\phi_{imref}).d\phi_{imref}$$

$$\boldsymbol{I_{ds} = I_{ds1} + I_{ds2}}$$

We have a unified expression of the drain current

THRESHOLD VOLTAGE BASED COMPACT MODEL

Short Channel Model

Valid in weak inversion!

evanescent analysis mode is used to get
expressions of the electrical potentials in the silicon film

$$\boxed{\psi(x,y)=\psi_{1D}(x)+\Delta\psi(\mathrm{x,y})}\,*$$

Correction factor: $\Delta\psi(\mathrm{x,y})=\dfrac{\mathrm{b}_1\,\mathrm{sh}\left(\dfrac{\pi}{\lambda_1}(L-y)\right)+\mathrm{c}_1\,\mathrm{sh}\left(\dfrac{\pi}{\lambda_1}y\right)}{\mathrm{sh}\left(\dfrac{\pi}{\lambda_1}L\right)}\cos\left(\dfrac{\pi}{\lambda_1}x\right)$ *

Ⓐ To explicitly calculate the drain current, we assume that for the correction factor, the current is dominant in x_{max} & y_{min}

Explicit expressions

$$\boxed{I_{ds}=-\mu\frac{W}{L}q\,n_i\,T_{si}\,u_t^2\,\frac{\exp\left(\dfrac{\psi_{s1}}{u_t}\right)-\exp\left(\dfrac{\psi_{s2}}{u_t}\right)}{(\psi_{s1}-\psi_{s2})}\exp\left(\frac{\Delta\psi(x_{\max},y_{\min})}{u_t}\right)\left(\exp\left(-\frac{V_{ds}}{u_t}\right)-1\right)}$$

* **X. Liang and Y. Taur,**
"A 2-D analytical solution
for SCEs in DG MOSFETs",
IEEE TED, vol.51, n°8, 2004.

THRESHOLD VOLTAGE BASED COMPACT MODEL

Short Channel Model

Compact Modeling

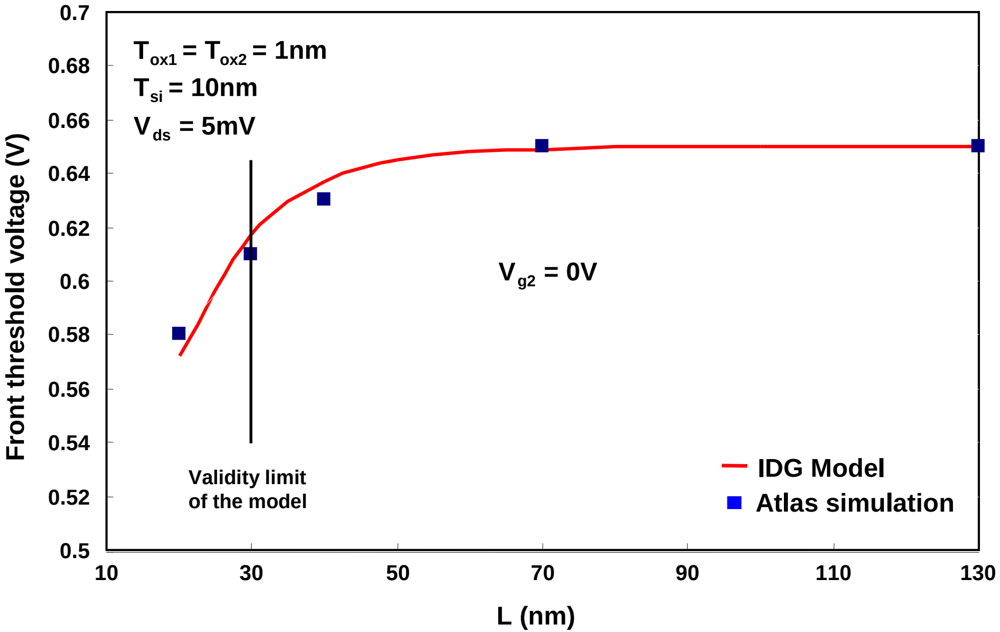
The drain current is written as the sum of a front & a back drain current

$$I_{dsi} = -\mu \frac{W}{L} n_i c_{oxi} u_t^2 (e^{\left(-\frac{V_{ds}}{u_t}\right)} - 1) e^{\left(\frac{V_{gi} - V_{thi}}{n_i u_t}\right)} e^{\left(\frac{\Delta\psi(x_{\max}, y_{\min})}{u_t}\right)}$$

We want to write it as:

$$I_{dsi} = -\mu \frac{W}{L} n_i \, c_{oxi} \, u_t^2 (e^{\left(-\frac{V_{ds}}{u_t}\right)} - 1) \, e^{\left(\frac{V_{gi} - V_{thi,sce}}{n_{i,sce} \, u_t}\right)}$$

By identification, we get explicit expressions of $V_{thi,sce}$ and of $n_{i,sce}$



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INTRODUCTION IN VERILOG-A

Unification of the different operating modes on the drain current

Unification in V_{gi}

$V_{offi}=\varepsilon_i(V_{gi}-V_{thi})$

$$\boxed{V_{gti}=2u_t n_i \ln\left[1+\frac{\exp\left(\frac{V_{gi}-V_{thi}-V_{offi}}{2u_t n_i}\right)}{1+2\exp\left(-\frac{V_{gi}-V_{thi}}{2u_t n_i}\right)}\right]}$$

Weak Inversion

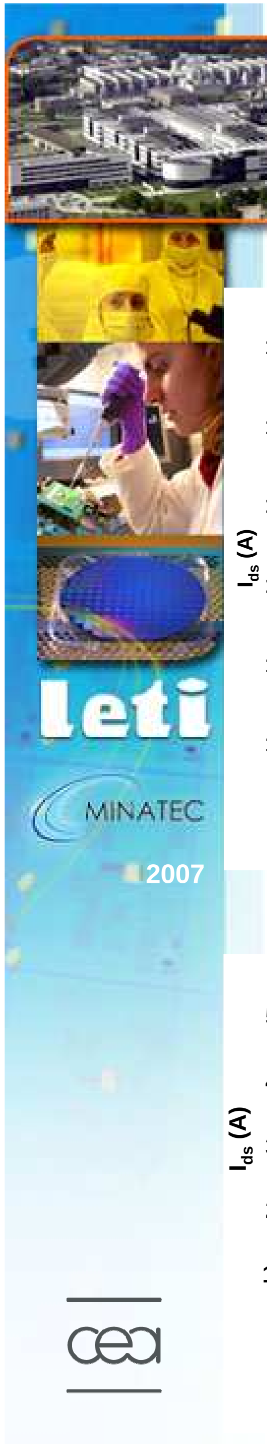
$$V_{gti}=u_t n_i \exp\left(\frac{V_{gi}-V_{thi}-\frac{V_{offi}}{2}}{u_t n_i}\right)$$

Strong Inversion

$$V_{gti}=V_{gi}-V_{thi}-V_{offi}$$

Unification in V_{ds}

$$\boxed{V_{dseff,i}=V_{dsat,i}-\frac{1}{2}\left[V_{dsat,i}-V_{ds}-\delta+\sqrt{\left(V_{dsat,i}-V_{ds}-\delta\right)^2+4\delta V_{dsat,i}}\right]}$$

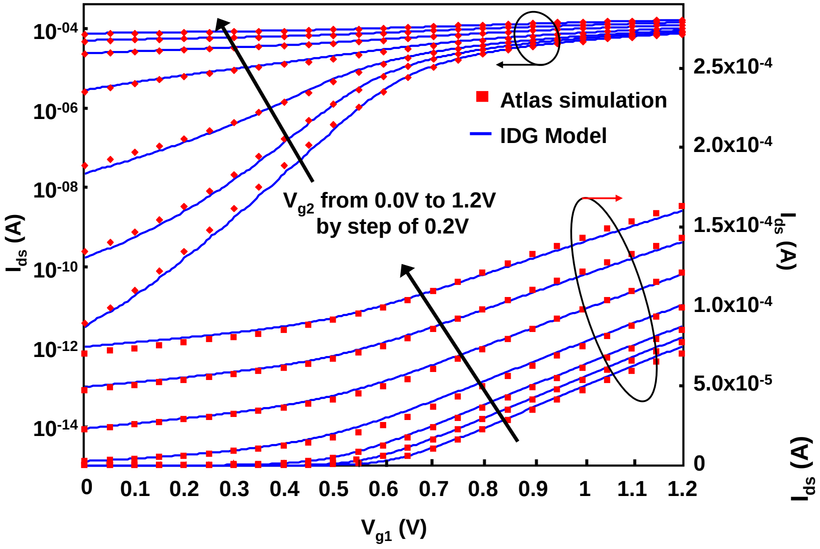


RESULTS

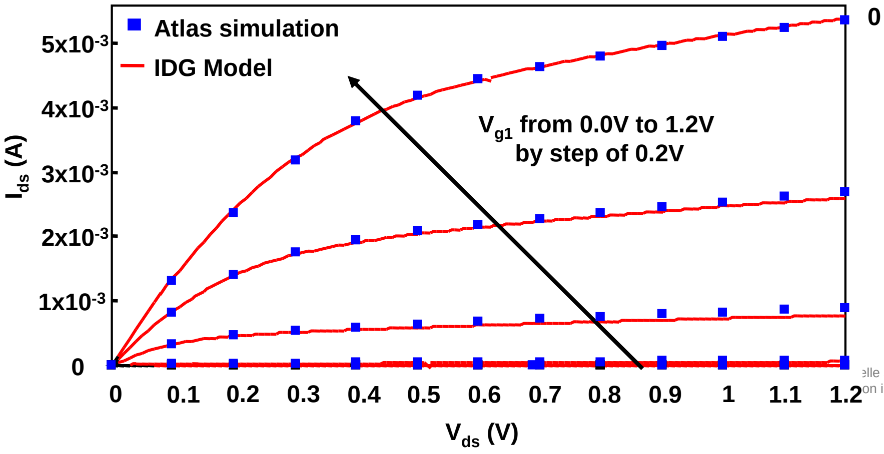
Short Channel Model

$T_{ox1}=T_{ox2}=1.2nm$
Tsi=10nm
L=30nm
W=1µm
µ=constant

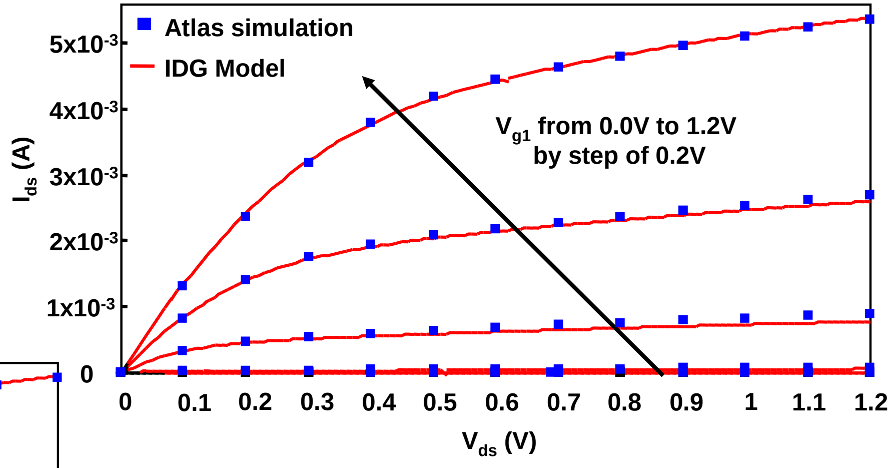
V_{ds} = 5 mV



V_{g2} = 0 V



V_{g2} = 1.2 V



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CONCLUSION & PROSPECTS

Our compact model takes into account independent gates

- Threshold voltage based compact model
- Explicit short channel effects
- Included effects: R_{series}, GIDL, gate leakage, mobility degradation…
- Results correspond very closely to numerical simulations

Effects to add

Quantum Effects

Ballistic Transport

THANK YOU FOR ATTENTION