

TCAD-based Process-Aware HSPICE Model Parameter Extraction

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Agenda

- **Need and Application of Process-Dependant SPICE Model Card**
- **Extraction Methodology**
- **Summary**

Example of the HSPICE model card

Process-Dependant model card

Process Parameter	Allowed Variation
<i>GOT</i> -Gate oxidation temperature	±10°C
<i>HD</i> -Halo implant dose	±1e12 cm ⁻²
<i>VtA</i> -Vt-adjust implant dose	±1e12 cm ⁻²
<i>dL</i>	±0.005μ

Nominal model card

```
.MODEL nch NMOS (
vth0 = 0.299
phin = 0.174
k1    = 0.442
eta0  = 0.757
. . . . .
```

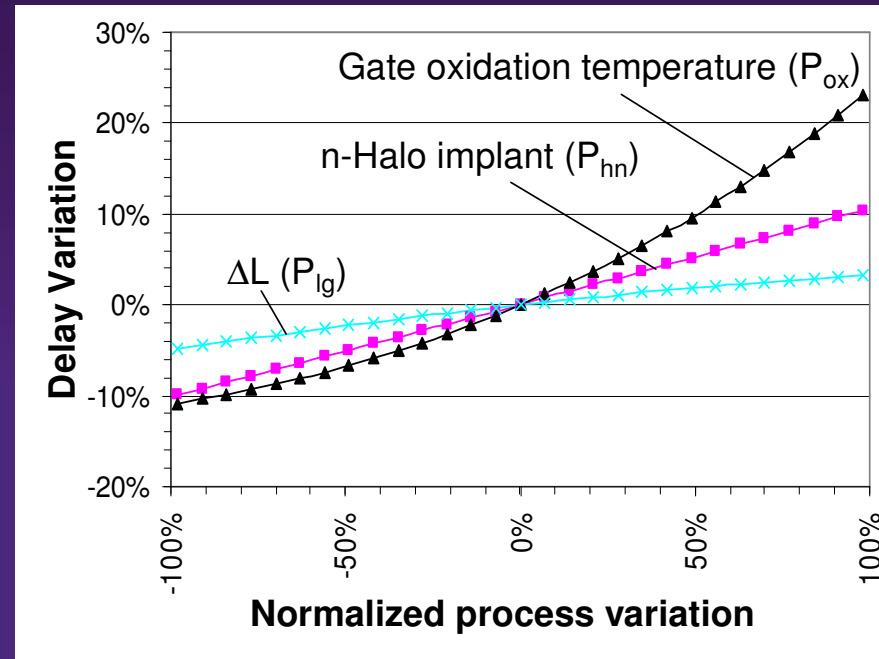
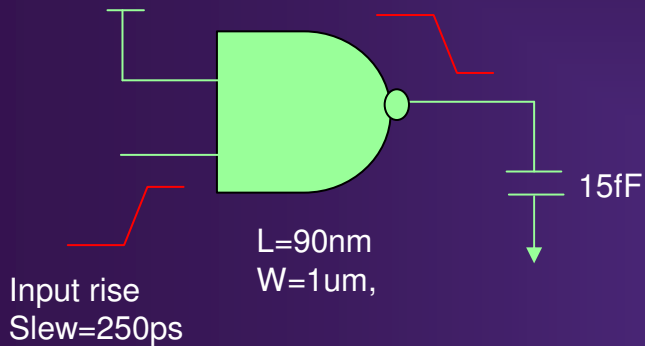


```
.param
dvth0=          +4e-3*GOT+3e-4*GOT2
                +3e-14*HD-4e-28*HD2
dphin=-4*dL+70*dL2
                -8e-5*GOT-2e-4*GOT2
                -5e-16*VtA-9e-27*VtA2-6e-14*HD+3e-27*HD2
dk1   =          +1e-6*GOT-3e-4*GOT2
                -3e-17*VtA-7e-27*VtA2+5e-15*HD-1e-26*HD2
deta0=          -1e-5*GOT+7e-4*GOT2
                -4e-15*VtA-1e-27*VtA2-7e-15*HD-4e-27*HD2
. . . . .
```



```
.MODEL nch NMOS (
vth0 = `0.299+dvth0`
phin = `0.174+dphin`
k1    = `0.442+dk1`
eta0  = `0.757+deta0`
. . . . .
```

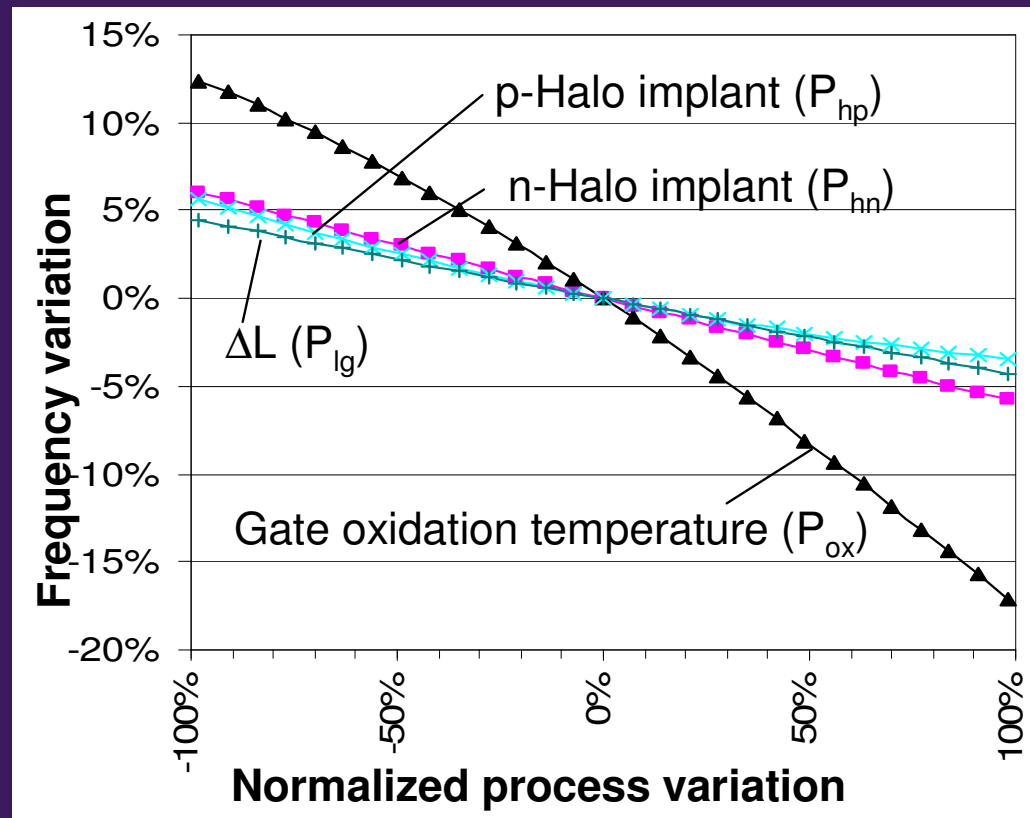
NAND Delay Variation and Sensitivity



- **Delay is most sensitive to T_{ox} variation .**
 - Varies from -10% to +24% as Δp_{ox} changes -100% to +100%
- **The response to gate length variation (ΔL) is relatively weak**
 - - 5% to +5% across the full range of ΔL variation.
- **Variation around nominal process is non-symmetrical**
 - -10 % vs 24% for min and max variation.

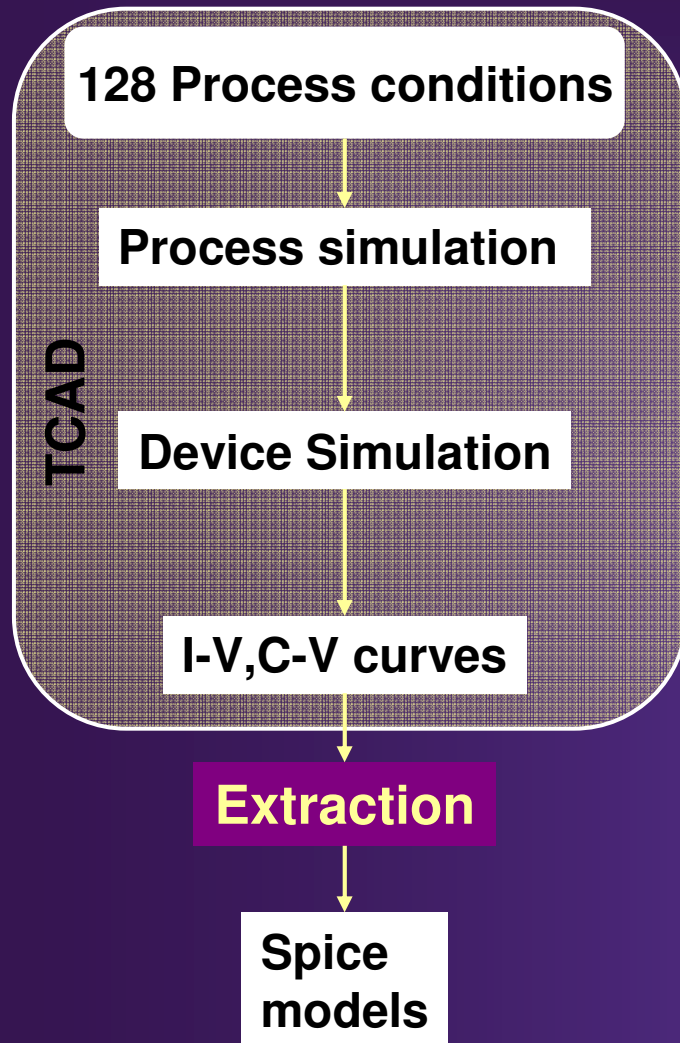
Ring Oscillator Frequency Variation

21 stage 2-INPUT NAND ring oscillator



- Frequency is most sensitive to T_{ox} variation.

Generation of Compact Spice Models



Nominal Condition:

Drawn gate Length = 90nm
Physical Gate Length = 65nm
N-Halo Dose Implant = $1.05e+13$
P-Halo Dose Implant = $1.4e+13$
N-Vt Adjust Implant = $6.0e+12$
P-Vt Adjust Implant = $7.0e+12$
Spike Temperature = 1050°C
Gate oxidation Temp = 900°C

•Process and device simulation decks are obtained from the calibration team

Problem Definition

$$\vec{P} = \vec{P}^{(1)} = (P_1, P_2, \dots, P_N)^T$$

P is the process condition vector

$$M_i = M^0_i + \sum_{j=1}^N (A^{(j)} \Delta \vec{P}^{(j)}) \quad | \quad i = 1 \div M$$

M is the model parameter
 A is the process coefficients

$$RMS(f, \vec{M}) = \sum_l \sum_k \left(\frac{f_{mes}(\vec{V}_k)_l - f_{sim}(\vec{V}_k, \vec{M})_l}{f_{mes}(\vec{V}_k)_l} \right)^2 =$$

$$\sum_l \sum_k \left(\frac{f_{mes}(\vec{V}_k)_l - f_{sim}(\vec{V}_k, \vec{M}^0, A^{(1)}, A^{(2)}, A^{(3)}, \Delta \vec{P}_l)}{f_{mes}(\vec{V}_k)_l} \right)^2$$

RMS error between TCAD (f_{mes})
 And extracted data (f_{sim}) over all
 the process conditions (l) and
 over all the Bias conditions (k)

$$F_{total}(\vec{M}) = F_{total}(\vec{M}^0, A^{(1)}, A^{(2)}, A^{(3)}) =$$

$$RMS(Id, \vec{M}) + RMS(Gm, \vec{M}) + RMS(Gds, \vec{M}) +$$

$$RMS(Cg, \vec{M}) + RMS(Cd, \vec{M}) + \Psi(\vec{M})$$

Goal function which provides
 process coefficients (A) and
 Nominal SPICE Model parameter
simultaneously

Example: how to find linear Process Coefficients

Step1

$$\begin{pmatrix} dvth0 \\ dphin \\ dk1 \\ deta0 \\ \dots \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \dots \end{pmatrix} * \begin{pmatrix} dL \\ GOT \\ VtA \\ HD \\ \dots \end{pmatrix}$$

Step2

$$\begin{pmatrix} dvth0 \\ dphin \\ dk1 \\ deta0 \\ \dots \end{pmatrix} = \begin{pmatrix} 0 & a1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \dots \end{pmatrix} * \begin{pmatrix} dL \\ GOT \\ VtA \\ HD \\ \dots \end{pmatrix}$$

.....
.....

StepN

$$\begin{pmatrix} dvth0 \\ dphin \\ dk1 \\ deta0 \\ \dots \end{pmatrix} = \begin{pmatrix} 0 & a1 & 0 & a2 \\ a18 & a29 & a46 & a9 \\ 0 & a42 & a30 & a31 \\ 0 & a33 & a16 & a24 \\ \dots \end{pmatrix} * \begin{pmatrix} dL \\ GOT \\ VtA \\ HD \\ \dots \end{pmatrix}$$

Summary

- **Process variables are built into compact spice models and accessible for circuit simulations.**
- **The core technology is an extraction engine based on calibrated TCAD simulations.**
- **Case studies demonstrated excellent quality of the modeling. Process impacts to simple circuits are explored.**