

Unified Approach to Bulk/SOI/UTB/s-DG MOSFET Compact Modeling

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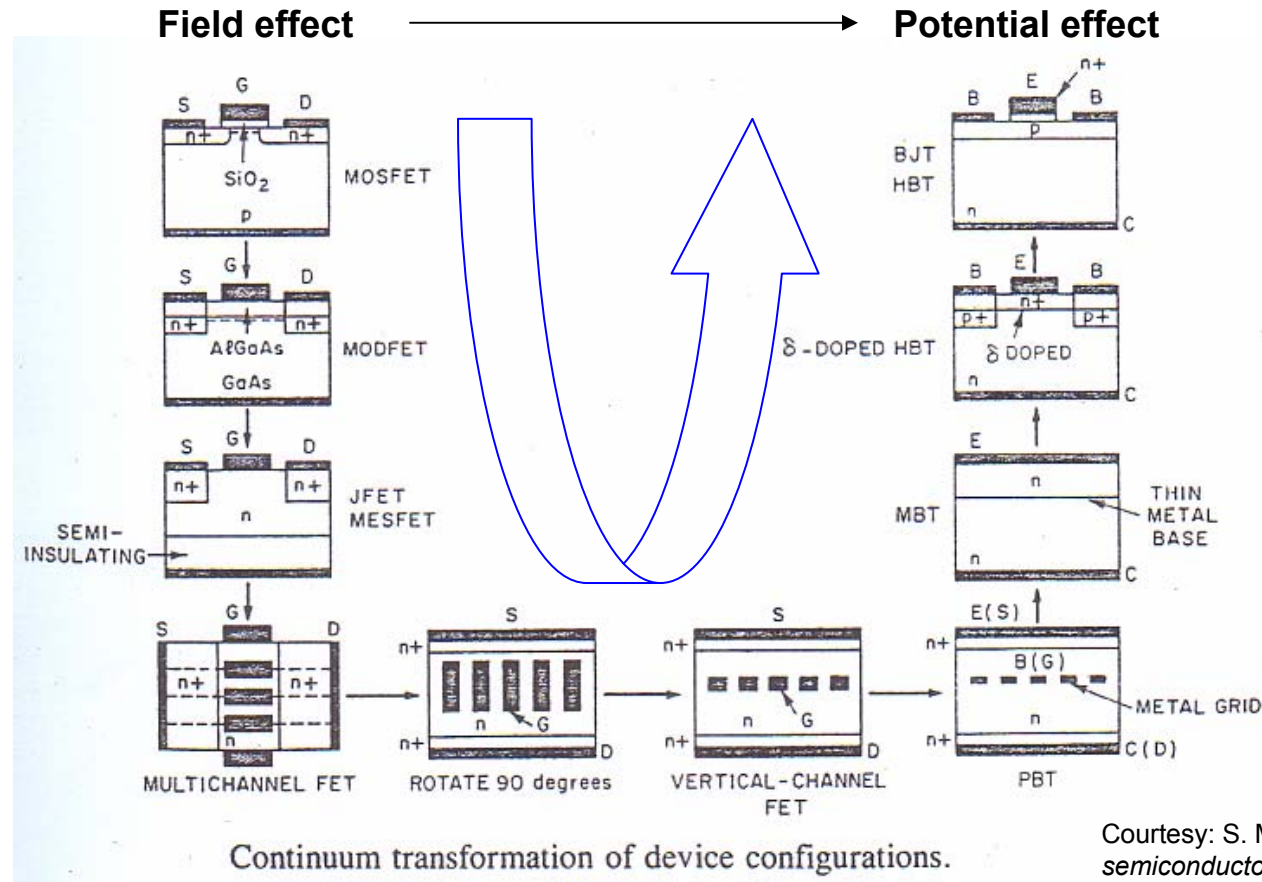
Presentation Outline

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- **Introductory question:** best models and approaches to various MOS structures and operations?
- **Unified view and unification of MOS models**
- **Unified regional approach**
- **Application and results**
 - ❑ Strained-Si heterostructure channel
 - ❑ Doped symmetric-DG
 - ❑ Undoped DG/SOI
 - ❑ *Latest:* Doped asymmetric-DG
- **Summary and conclusions**

Continuum Transformation: FET to BJT

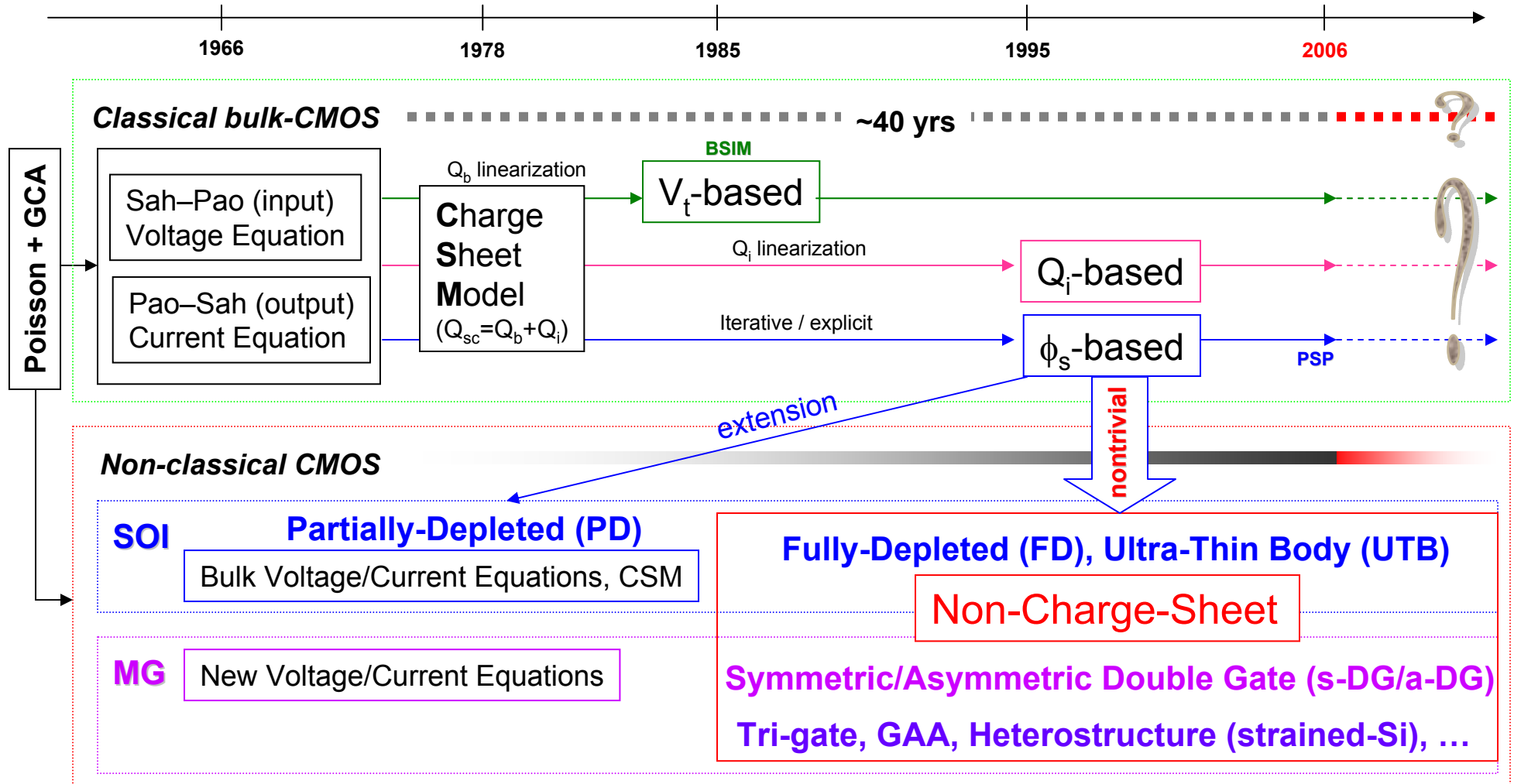


Similar transformation from **classical bulk-MOS** to **non-classical SOI/MG MOSFETs**?

MOSFET Compact Models: History and Future

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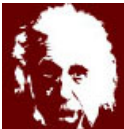


Motivation: Unification of MOSFET Models

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- ❑ After ~40 years, **bulk**-MOS compact modeling ‘goes back’ to the original (ϕ_s) formulation/solution, mainly because “ V_t ” approach cannot meet the requirement of current technologies.
- ❑ As bulk-CMOS scaling is approaching its limit ($\ll 40$ yrs?) and **non-classical** CMOS emerges, do we want to ‘**re-start**’ from new formulations due to **non-extendable** bulk formulation? Or, do we want to build non-classical models ‘**in parallel**’ with bulk models?
- ❑ As a device (geometry/layer) dimensions and (physical/electrical) parameters vary, its operations change seamlessly; so should the models describing its characteristics be.
- ❑ **Motivation**: A ‘**unified**’ MOS model with **seamless** transitions across device types and operations.



Politics is for the present, but an equation is something for eternity.

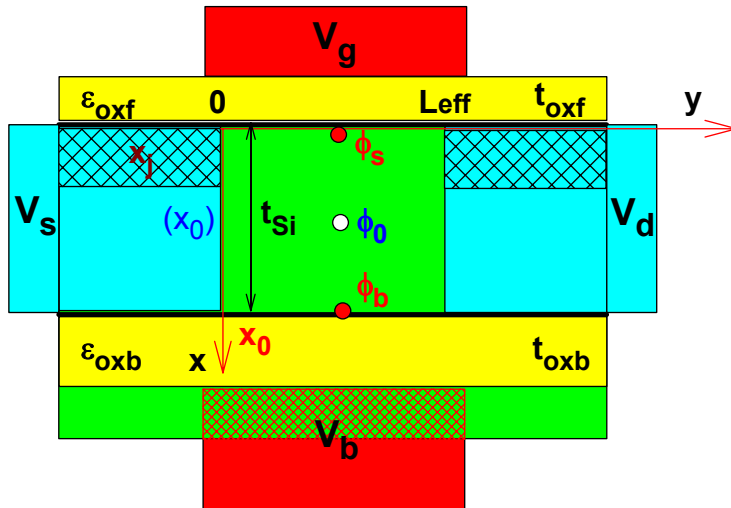
Albert Einstein

The best of Einstein’s theory is not only a brand *new* theory, but one that includes *old* (Newton’s) theory as a special case.

Unified View of a MOSFET with Two Gates

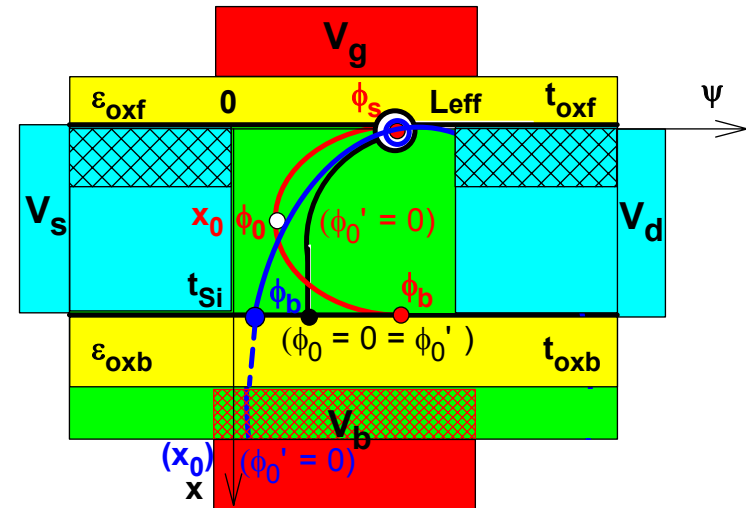
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Key physical parameters

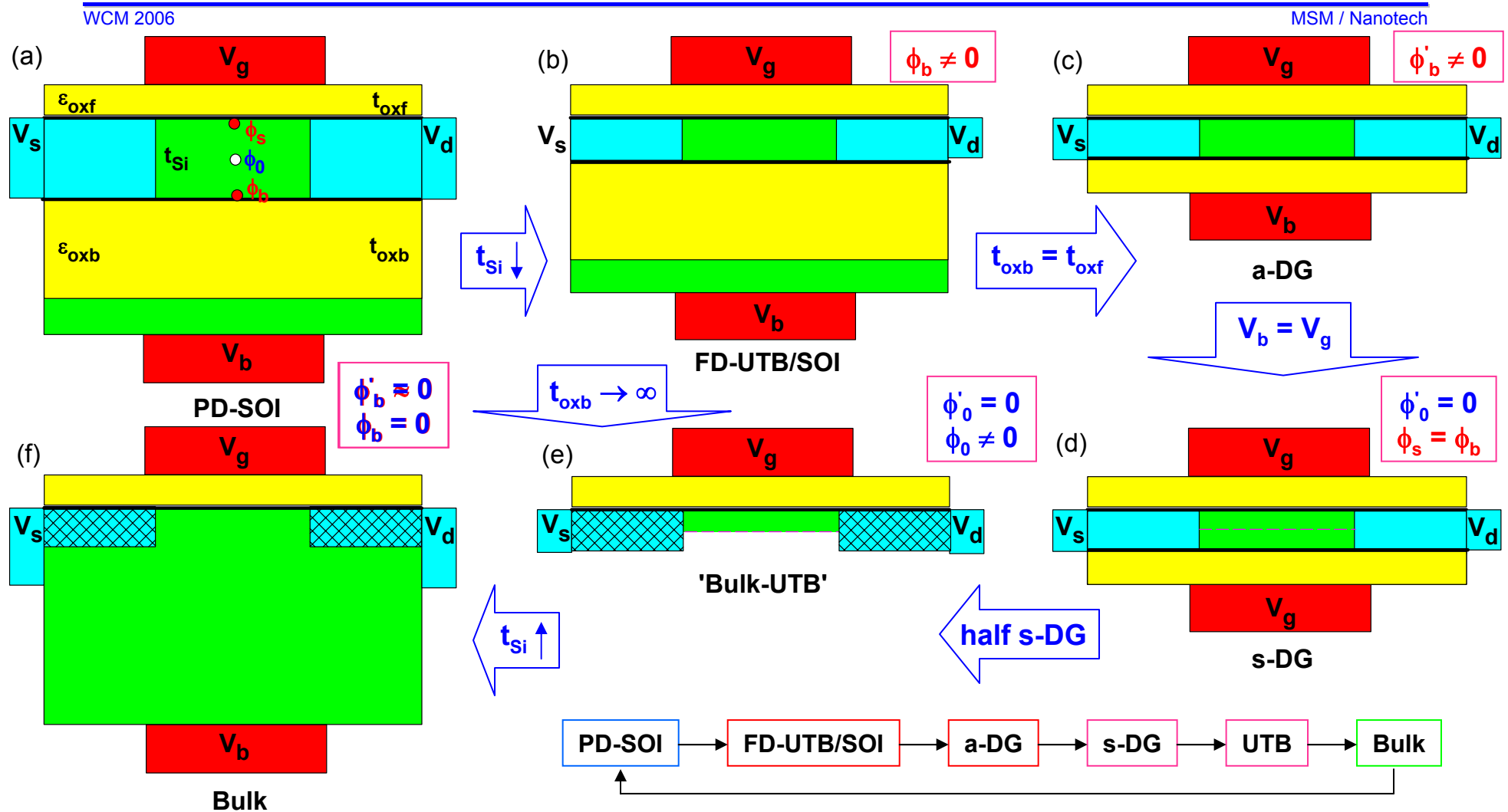
- Channel thickness (t_{si}) and doping (N_{ch})
- Front/back oxide thickness (t_{oxf}/t_{oxb})
- Front/back gate dielectric constant ($\epsilon_{oxf}/\epsilon_{oxb}$) and flat-band (V_{FBf}/V_{FBb})
- Others: channel length (L_{eff}), junction depth (x_j), over/under-lap (ΔL), and doping (N_{sd})



Different structures/operation

- Bulk: $\phi_b = 0, \phi'_b = 0$
- PD-SOI: $\phi_b = 0, \phi'_b \approx 0$
- FD-SOI: $\phi_b \neq 0, \phi'_b \neq 0$
- a-DG: $\phi_b \neq 0, \phi'_b \neq 0$
- s-DG: $\phi_0 \neq 0, \phi'_0 = 0$

Seamless Transformation and Unification of MOSFETs



Generic Voltage Equations for DG/SOI/Bulk MOSFET

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□ Poisson Equation



(First integral)

□ Field Equation

$$\frac{d^2\psi}{dx^2} = -\frac{\rho}{\epsilon_{Si}} = -\frac{q(p-n+N_D-N_A)}{\epsilon_{Si}} = \frac{q}{\epsilon_{Si}}(n-p+N_A-N_D)$$

$$= \frac{qN_A}{\epsilon_{Si}} \left[e^{(\psi-2\phi_F-V_c)/v_{th}} - e^{-\psi/v_{th}} + 1 - e^{-(2\phi_F+V_c)/v_{th}} \right] \equiv \frac{qN_A}{\epsilon_{Si}} G(\psi, V_c)$$

$$E_s^2 = E_0^2 + F_s^2$$

+

$$F_s(\phi_s, \phi_0, V_c) = \pm \sqrt{2qN_A/\epsilon_{Si}} \left[\int_{\phi_0}^{\phi_s} G(\psi, V_c) d\psi \right]^{1/2} \quad (\phi = \phi/v_{th})$$

$$= \pm \sqrt{2qN_A/\epsilon_{Si}} \left\{ v_{th} \left[e^{-\phi_s} - e^{-\phi_0} + (\phi_s - \phi_0) \right] + v_{th} e^{-(V_c-2\phi_F)} \left[e^{\phi_s} - e^{\phi_0} - (\phi_s - \phi_0) \right] \right\}^{1/2}$$

(p)
(N_A)
(n)
(N_D)

□ Gauss' Law (boundary conditions)

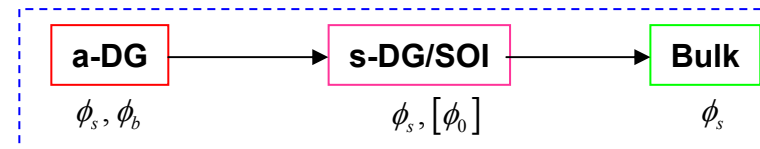
$$E_s = -\phi'_s = -\frac{\epsilon_{oxf}}{\epsilon_{Si}} \frac{V_{gf} - \phi_s}{t_{oxf}}, \quad (V_{gf} \equiv V_g - V_{FBf})$$

$$E_0 = E_b = -\phi'_b = +\frac{\epsilon_{oxb}}{\epsilon_{Si}} \frac{V_{bf} - \phi_b}{t_{oxb}}, \quad (V_{bf} \equiv V_b - V_{FBb})$$

||

$$\psi(0, y) = \phi_s(y), \quad E_x(0, y) = E_s(y) = -\phi'_s(y)$$

$$\psi(x_0, y) = \phi_0(y), \quad E_x(x_0, y) = E_0(y) = -\phi'_0(y)$$

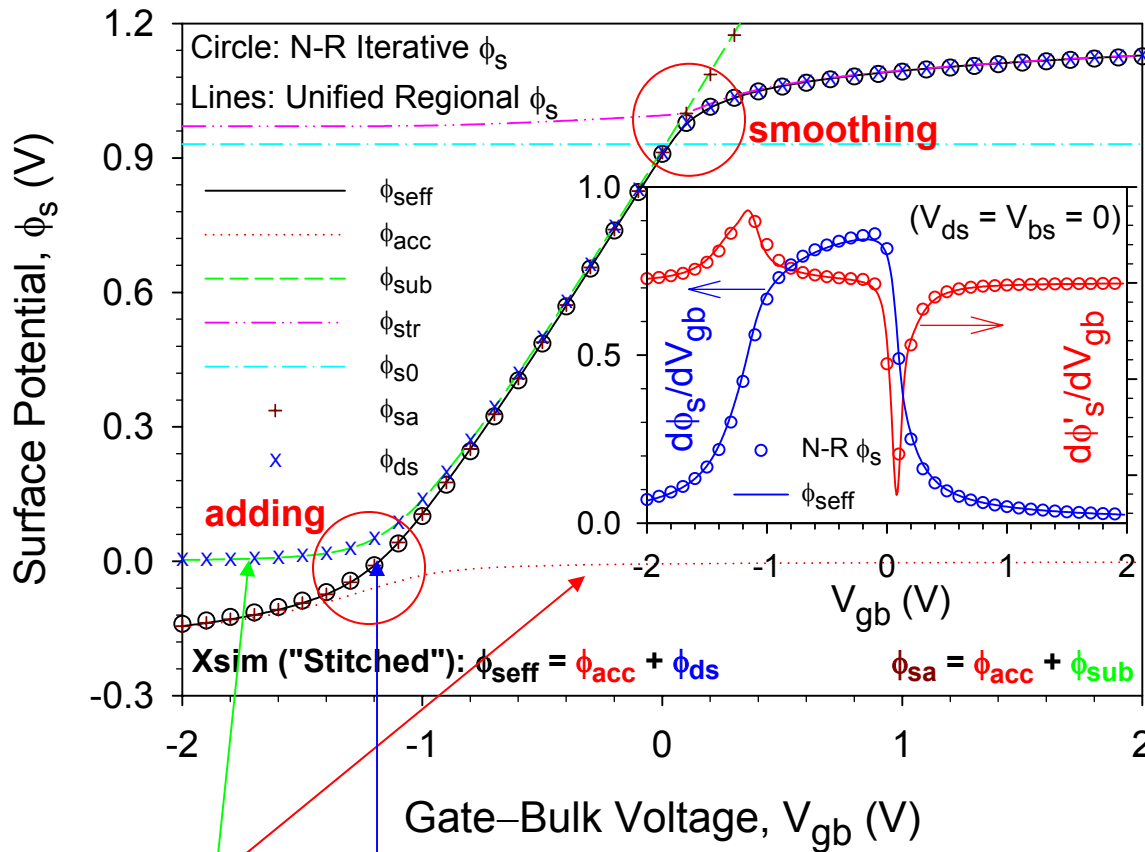


□ Voltage Equations (second integral not possible for doped channel)

Essence of the Unified Regional Approach

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$$\phi_s \approx \begin{cases} \phi_{cc} = V_{gb} - V_{FB} + 2v_{th}\mathcal{L}\{w\} & V_{gb} < V_{FB} \\ \phi_{dd} = \left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{gb} - V_{FB}}\right)^2 & V_{FB} < V_{gb} < V_t \\ \phi_{ss} = \phi_{s0} + V_{cb} + \Delta & V_{gb} > V_t \end{cases}$$

$$\phi_{s,eff} = \begin{cases} \phi_{acc} = V_{gbr} + 2v_{th}\mathcal{L}\{w\} & V_{gb} < V_{FB} \\ \phi_{sub} = \left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{gbf}}\right)^2 & V_{FB} < V_{gb} < V_t \\ \phi_{str} = \phi_{s0} + V_{cb} + \Delta_{eff} & V_{gb} > V_t \end{cases}$$

ϕ_s at $V_{gb} = V_{FB}$ is not solved exactly, but two pieces are “**stitched**” (rather than “**glued**”) to form a single-piece (ϕ_{seff}) seamlessly

“Pulled” to zero – no effect outside the region

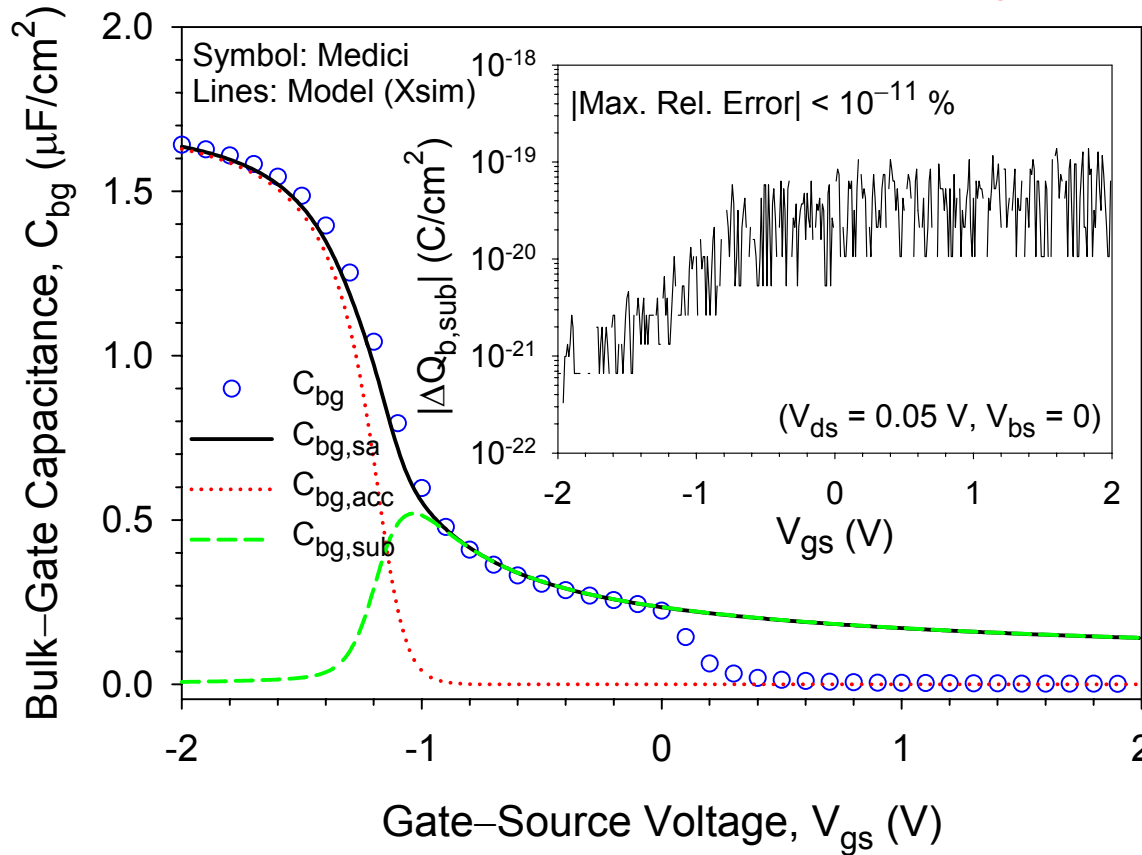
“Glued”/iterative solution requires to maintain all the terms in the equation

Unified Regional Bulk-Charge Model

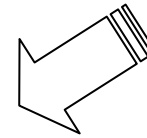
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Other CSM: Right-hand side valid for $V_{gb} \geq V_{FB}$



$$|\Delta Q_{b,sub}| = |Q_{b,sub} - Q_{b,sub1}|$$



Difference between the left-hand and right-hand side of the voltage equation

$$V_{gb} - V_{FB} \equiv V_{gbr} + V_{gba}$$

$$\phi_{sa} = \phi_{acc} + \phi_{sub}$$

$$Q_{sc} = -C_{ox} (V_{gb} - V_{FB} - \phi_{sa})$$

$$= -C_{ox} \left[\underbrace{(V_{gbr} - \phi_{acc})}_{Q_{b,acc}} + \underbrace{(V_{gba} - \phi_{sub})}_{Q_{b,sub1}} \right]$$

$$= Q_{b,acc} + Q_{b,sub}$$

$$Q_{b,acc} \equiv -C_{ox} (V_{gbr} - \phi_{acc})$$

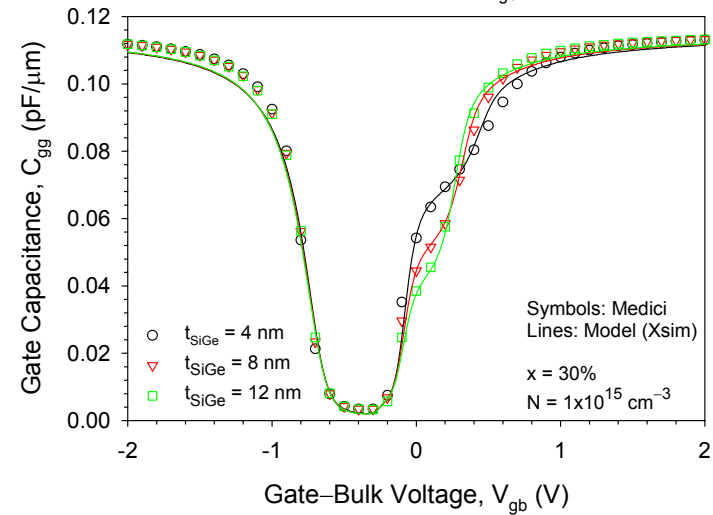
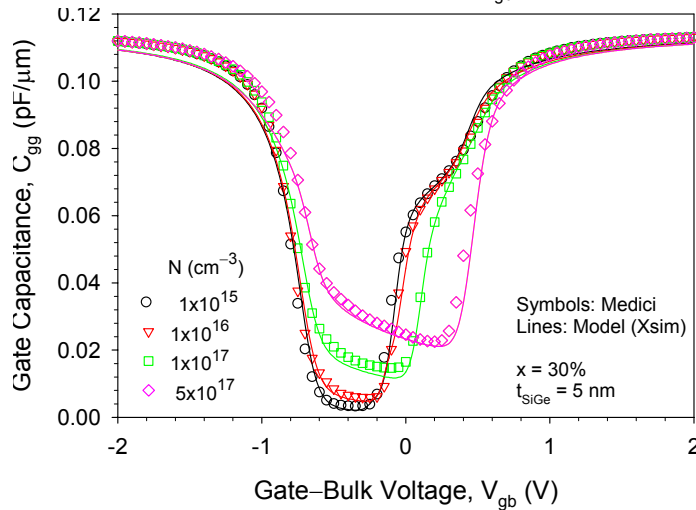
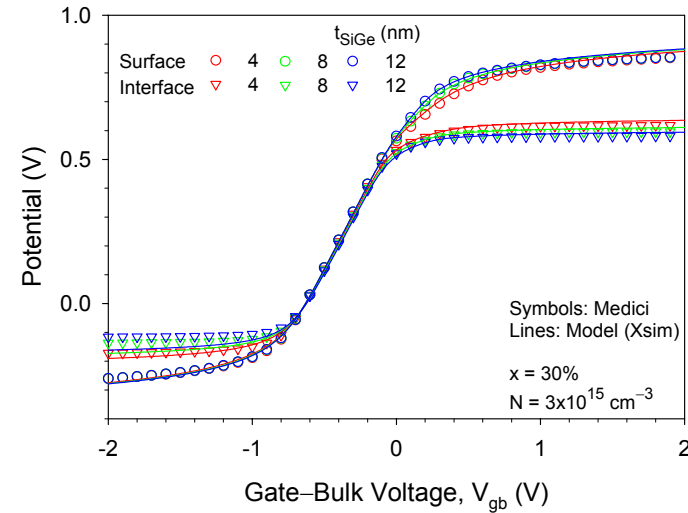
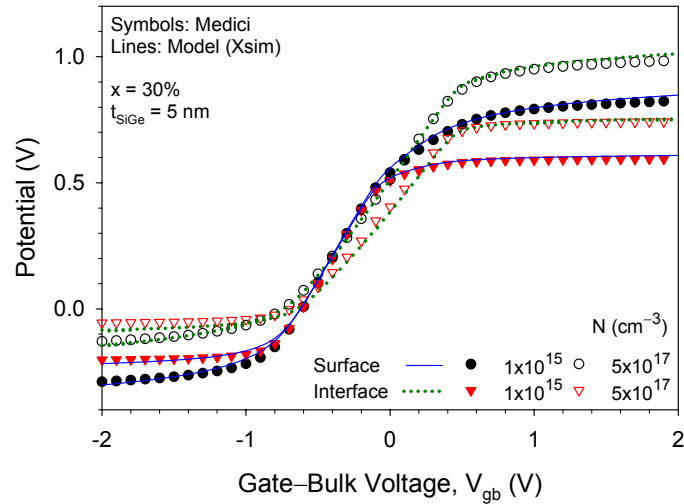
$$Q_{b,sub} \equiv -C_{ox} (V_{gba} - V_{gbf} + \gamma \sqrt{\phi_{sub}})$$

Extending to strained-Si/SOI/DG ...

Unified Regional Approach Applied to Strained-Si

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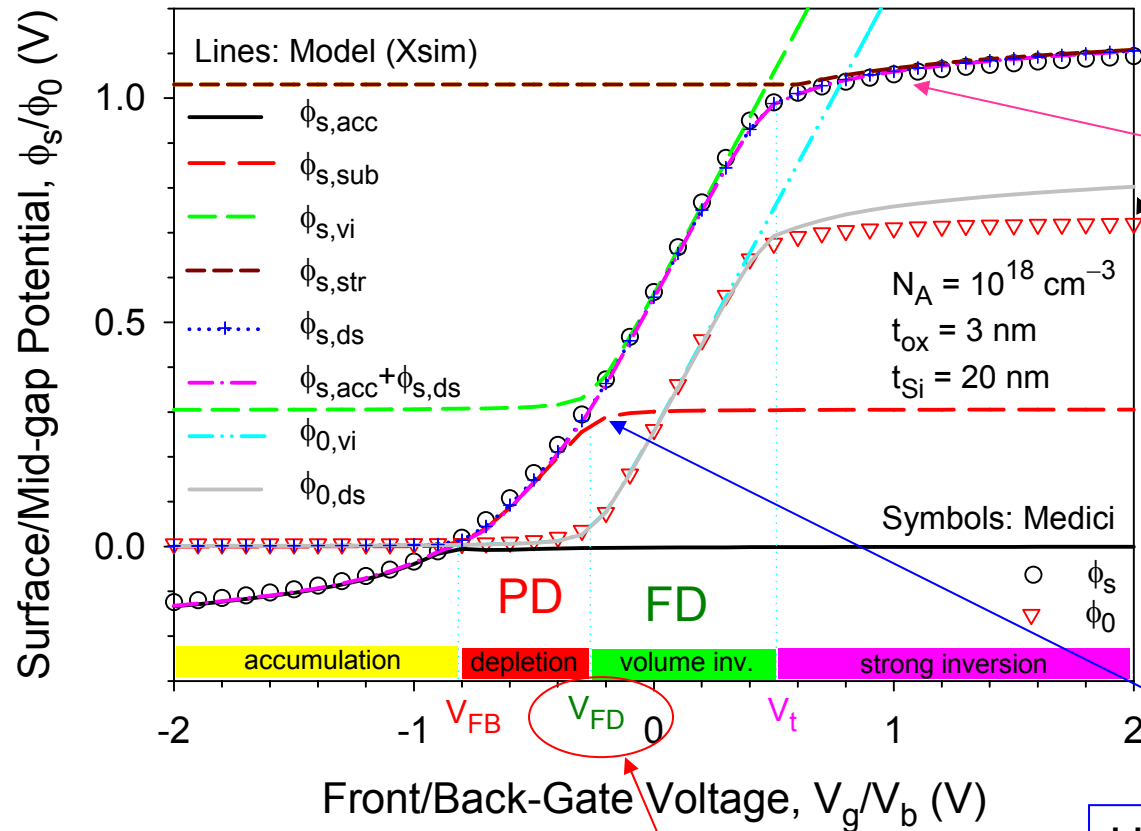
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Doped s-DG: Explicit Unified Regional Solutions

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‘Strong-inversion’ regional solution assuming channel full depletion

Inaccuracy in mid-gap potential has minimum effect on ϕ_s

Modeled physically

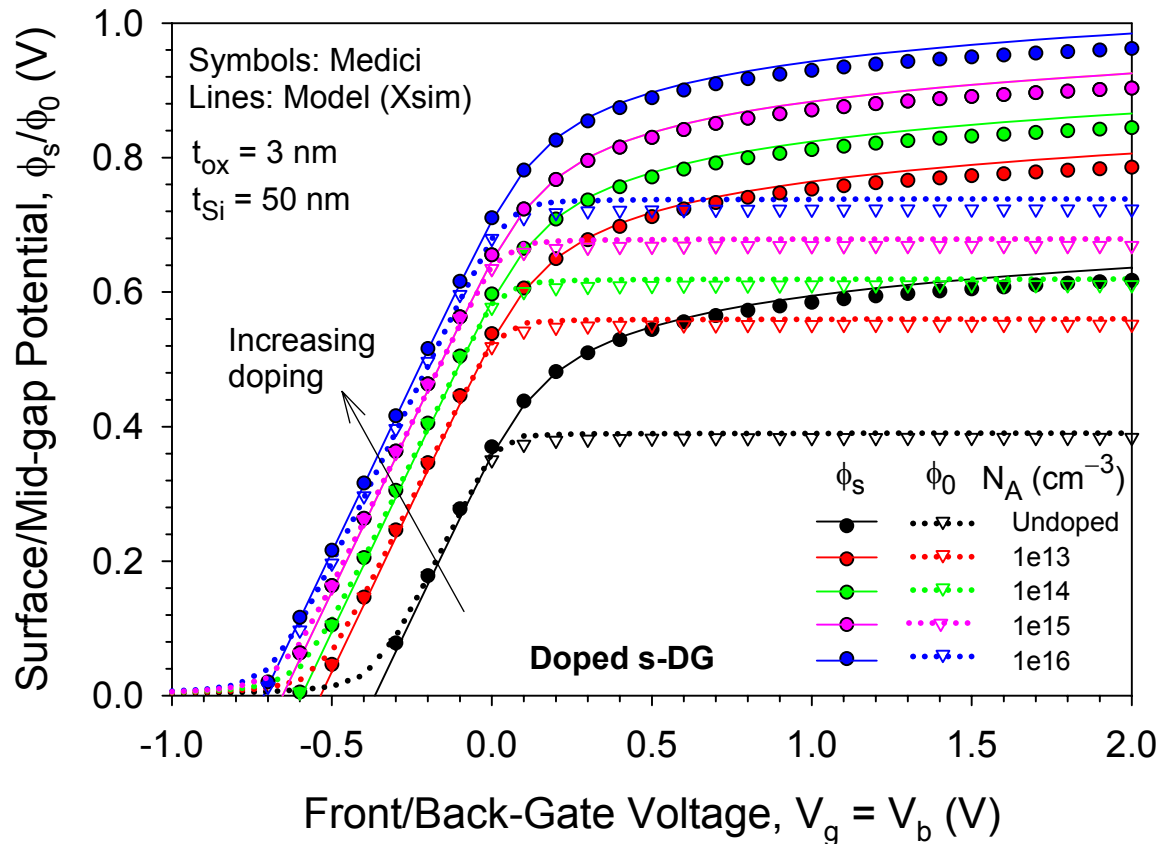
Unified regional solutions from ‘depletion’ to ‘volume inversion’

(See: WCM2006 poster by Karthik)

Doped s-DG: Doping Scaling – Doped to Undoped

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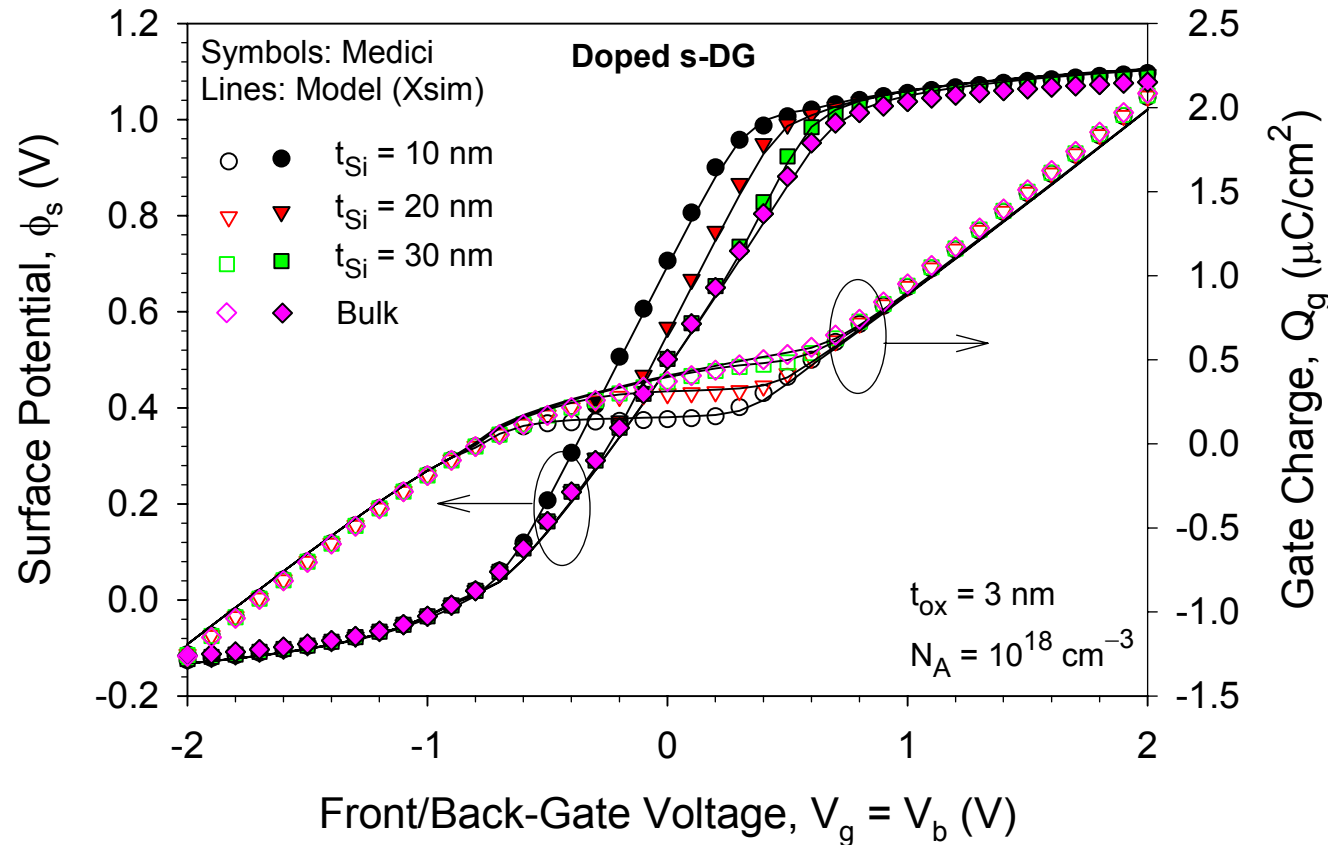


- Continuous** and seamless scaling with channel doping
- Essential** for accurate modeling for ‘undoped’ channel – with low ‘**unintentional**’ doping which, if not modeled, will lead to mV error in ϕ_s

Doped s-DG: Channel Thickness Scaling – UTB to Bulk

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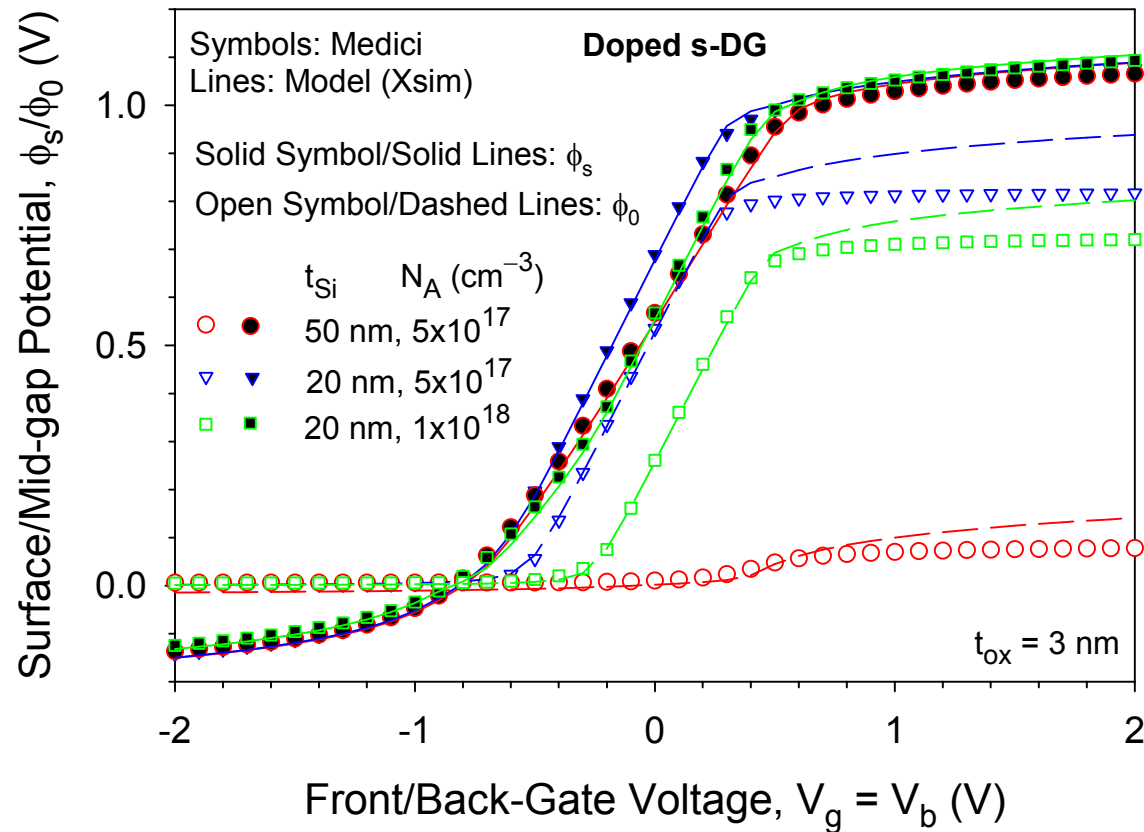
- Continuous scaling with channel thickness
- Unified model with seamless transition from UTB/DG to bulk MOSFETs

Doped s-DG: Doping & Channel Thickness Variations

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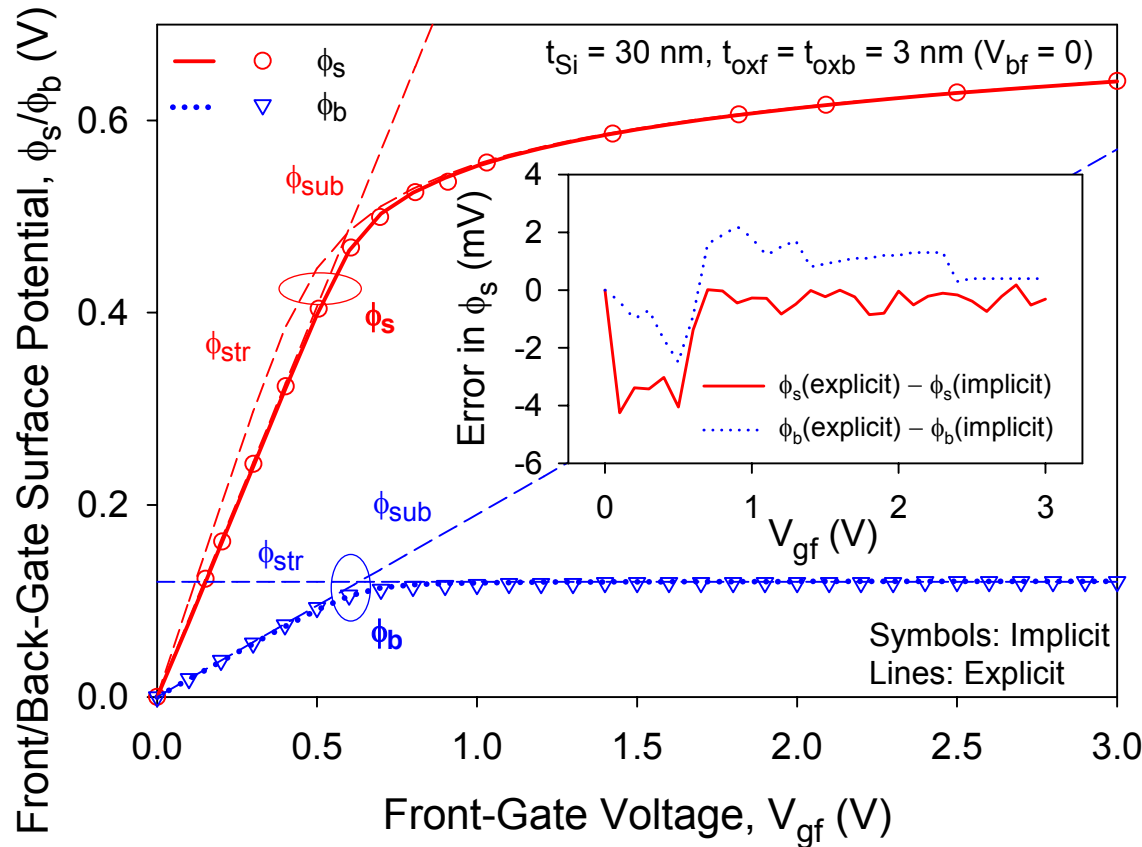
Comparison for t_{Si} (circle/triangle) and N_A (triangle/square) variations



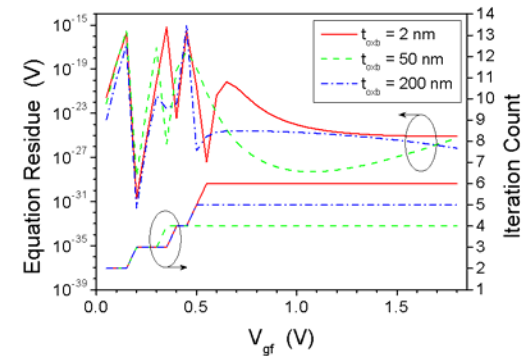
Undoped DG: Explicit Unified Regional Solutions

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Explicit regional solutions scalable with layer/bias



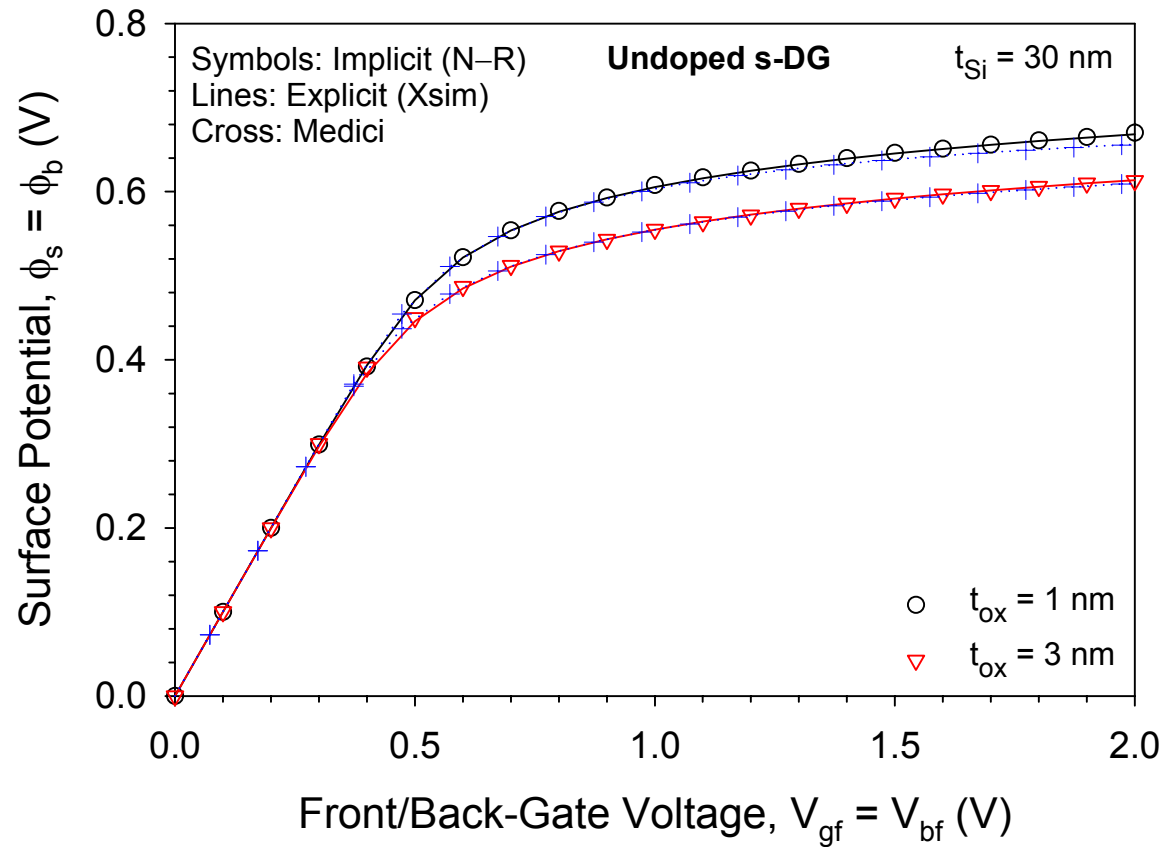
- ❑ **Implicit generic DG solutions are available**
- ❑ **Our Newton-Raphson solutions need 2~6 iterations to reach femto-V accuracy**
- ❑ **Explicit regional solutions are derived with mV accuracy**

Undoped s-DG: Explicit – Implicit – Numerical

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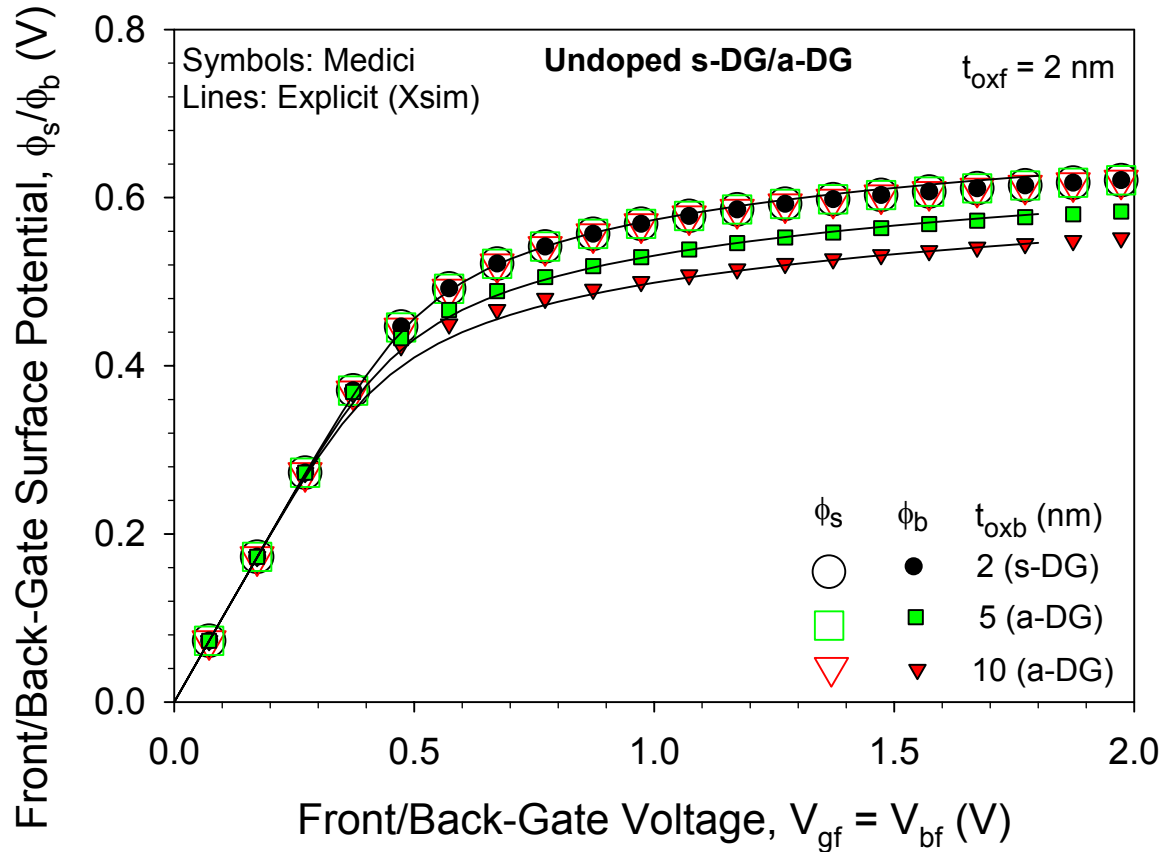
Comparison of **explicit** solution with **iterative** and **numerical** solutions



Undoped s-DG: Back Oxide Scaling – s-DG to a-DG

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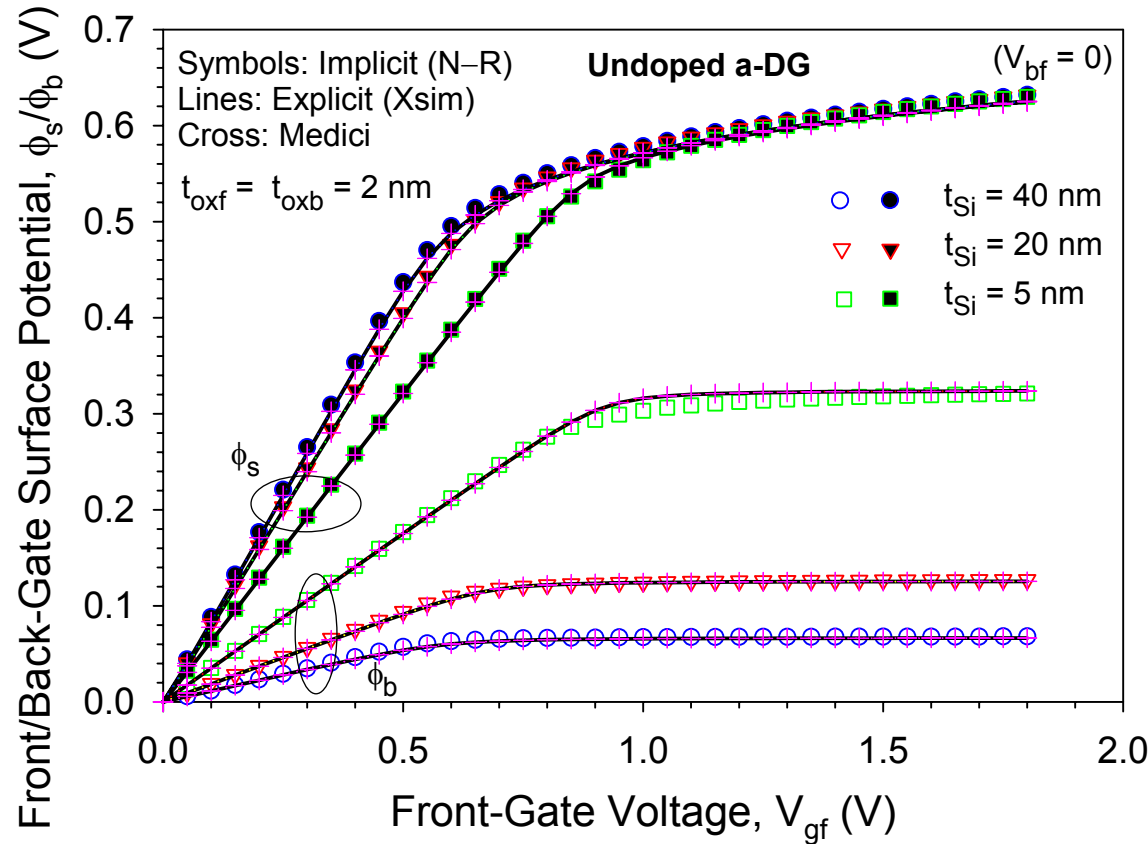


- Continuous scaling and transition from symmetric to asymmetric DG
- Asymmetry due to back-gate oxide thickness (t_{oxb}) variation ($V_g = V_b$)
- Comparison with numerical (Medici) solutions

Undoped a-DG: Channel Thickness Scaling

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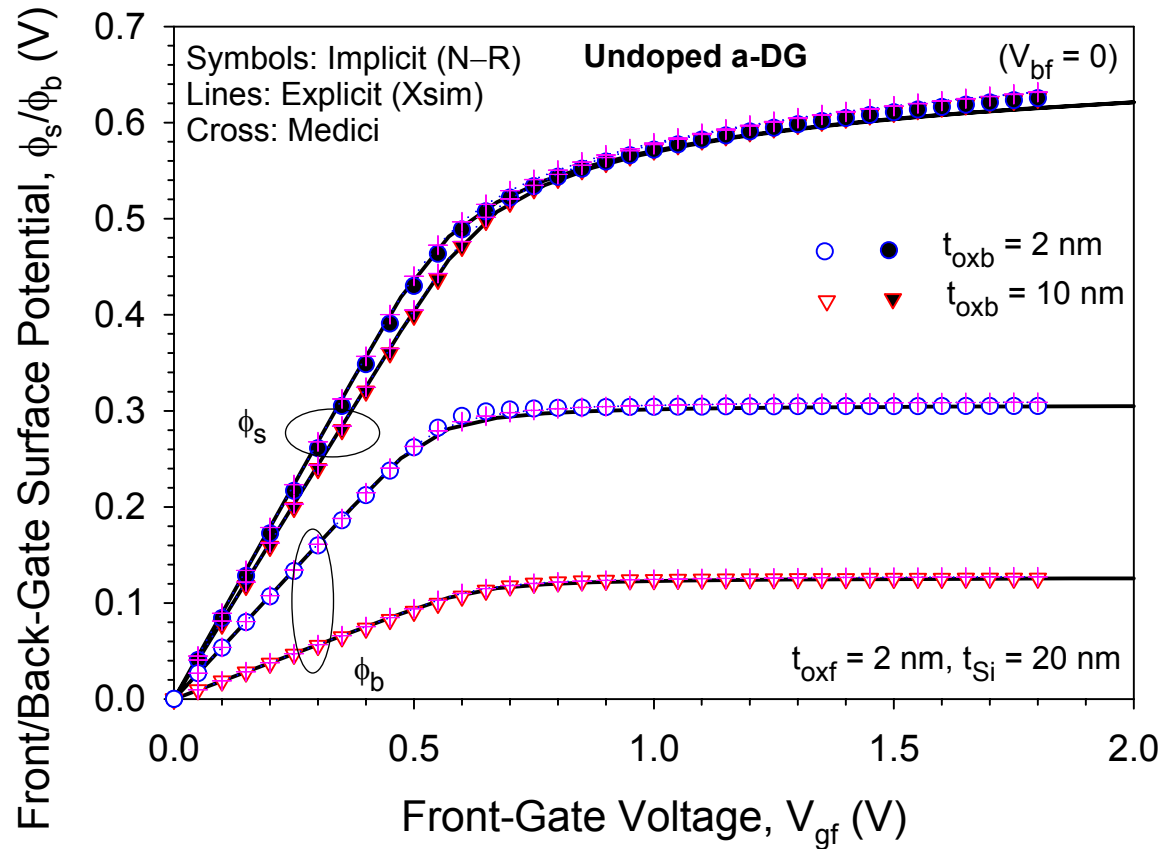


- Continuous** channel thickness scaling
- Asymmetry** due to single-gate bias (V_g) sweeping ($V_{bf} = 0$)
- Explicit** solution compared with **implicit** and **numerical** solutions

Undoped a-DG: Back Oxide Thickness Scaling

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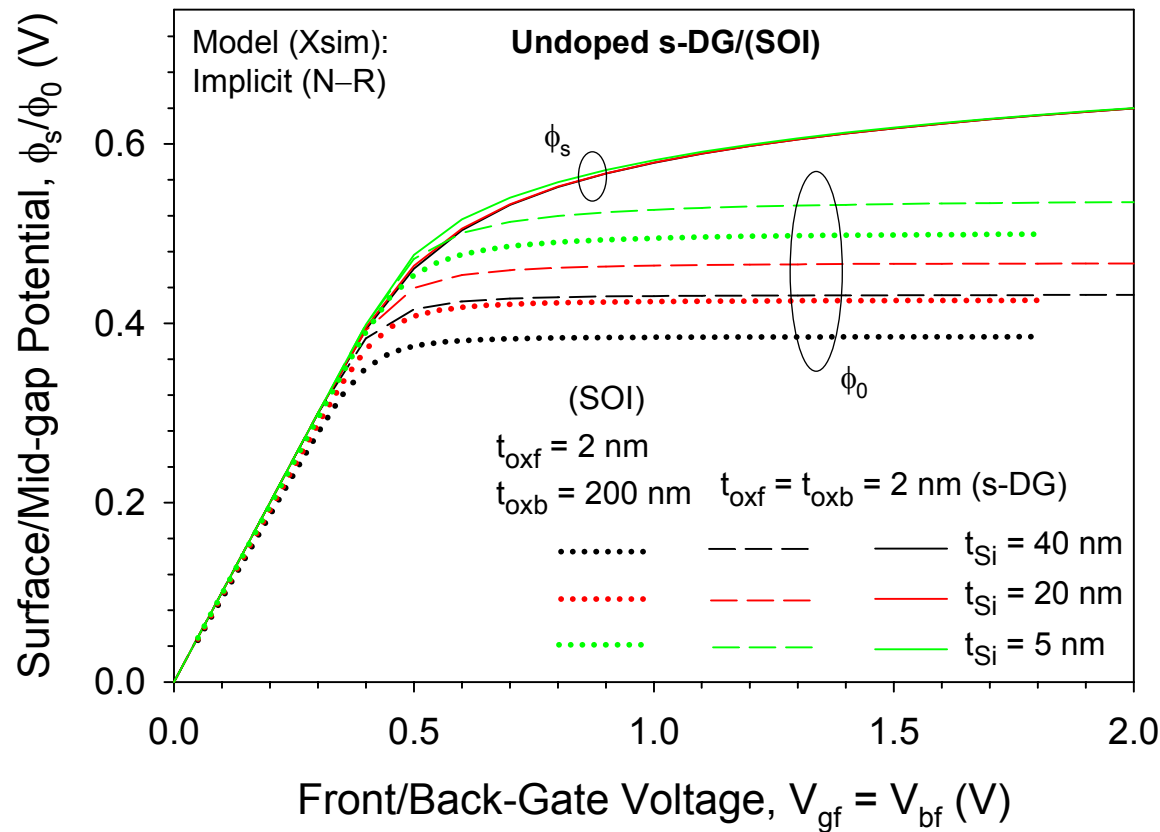


- Continuous** back-gate oxide thickness scaling
- Asymmetry** due to single-gate bias (V_g) sweeping ($V_{bf} = 0$)
- Explicit** solution compared with **implicit** and **numerical** solutions

Undoped s-DG: Channel Thickness Scaling – s-DG to SOI

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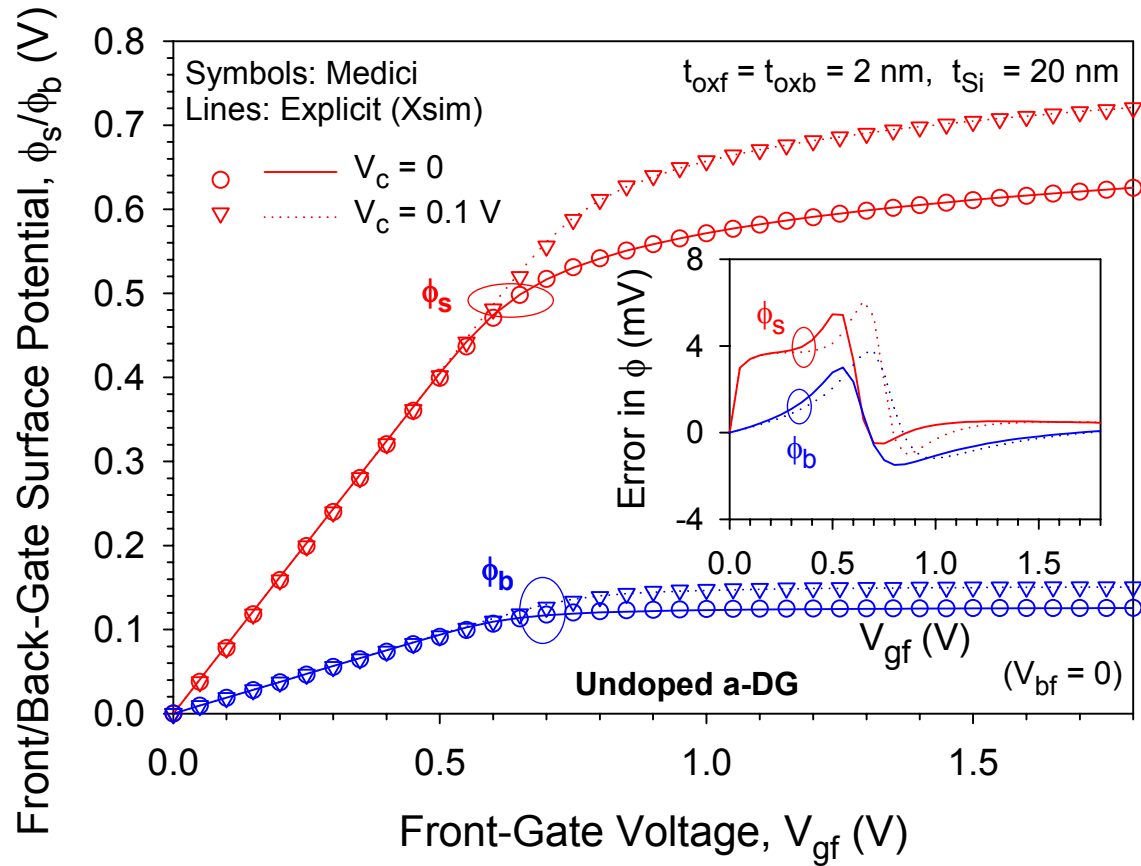


- Continuous channel thickness scaling
- Comparison between s-DG and 'SOI'
- Implicit N-R solution (difficult to converge as t_{oxb} approaches t_{oxf})

Undoped a-DG: Channel Voltage Variation for MOSFETs

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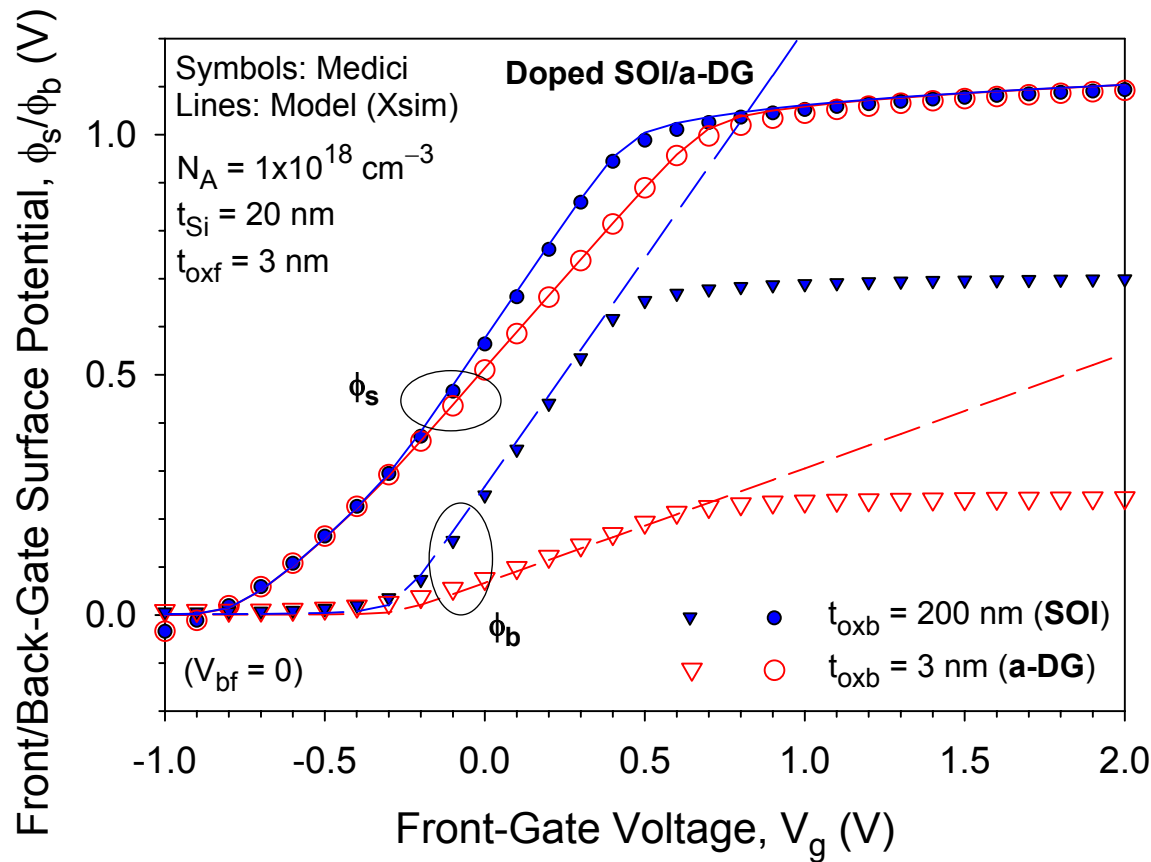
- Undoped a-DG with non-zero channel voltage ($V_c \neq 0$)
- Accurate ϕ_s and ϕ_b solutions needed for **MOSFET terminal current** evaluated at the source $\phi(V_s)$ and drain $\phi(V_d)$ ends
- Explicit** solution compared with **numerical** solution, showing **$\sim \text{mV}$** error for application to **MOSFETs**

Doped a-DG/UTB-SOI: Regional Solutions

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Seamless transition from a-DG to SOI



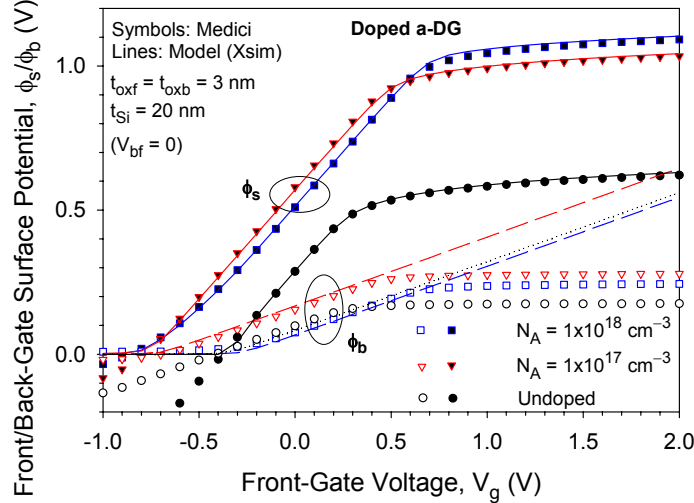
- ❑ The most challenging case: **doped a-DG & UTB/SOI** (known to be **non-integrable!**)
- ❑ Demonstrated physical/regional solutions in **depletion** and **volume inversion** regions, with **seamless** transitions in t_{oxb} , t_{Si} , N_A , V_b variations, validated by Medici
- ❑ Final challenge: **accurate** ϕ_b solution in **strong inversion!**

Seamless Transitions: Doping, Thickness, Bias Scaling

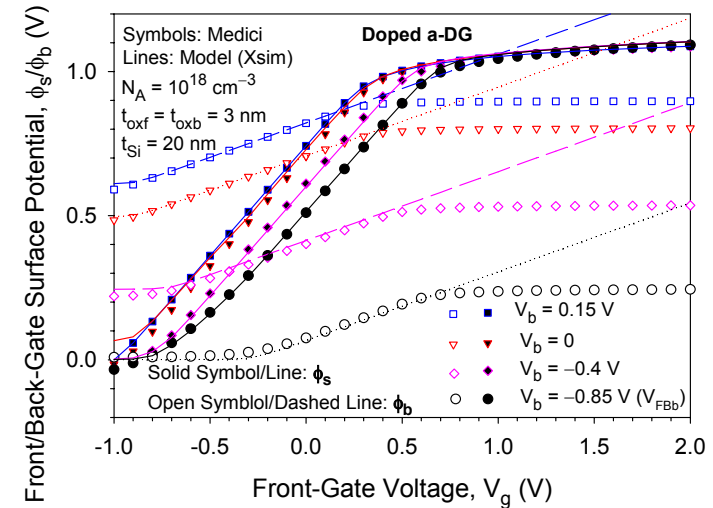
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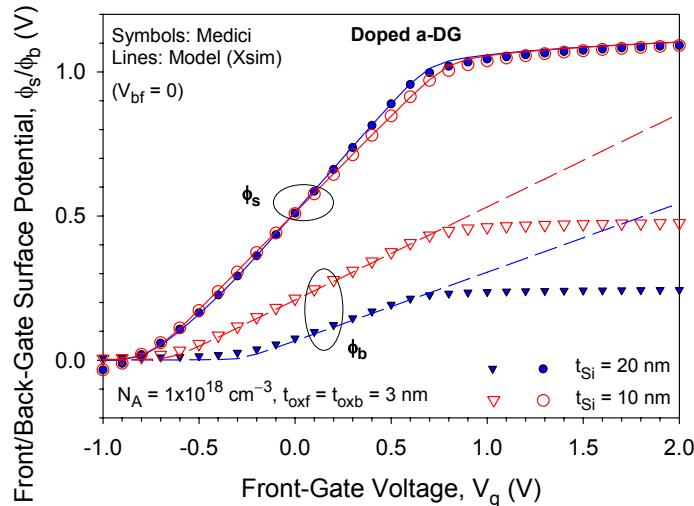
Doped to undoped



Back-bias scaling



DG: FD to PD



Latest results → conclusion / vision

- ☐ **Unified regional solution: the only 'solution' to future generation non-classical MOSFETs?**
- ☐ **Close to the 'final' ultimate solution: Unification of MOS models**

Summary and Conclusions

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- ❑ **What is the best modeling approach?** — from historical bulk-MOS development to future generation non-classical MOS structures/operations
- ❑ **Classical bulk ϕ_s -based formulation** — non-extendable to DG/non-CSM
- ❑ **Unified regional solutions** — feasible for constructing complete solutions for non-classical MOS with structural/operational variations and seamless transitions, which also includes bulk-MOS (and converges to the simplest V_t -based formulations)
- ❑ **Model development** — to tackle the ‘future’ problem, now; rather than re-starting or getting around or doubling the efforts. **Key:** the approach
- ❑ **Goals and Vision** — **Unification** of MOS models with the *unified regional approach* within one model infrastructure and seamless transitions across device types and operations

Acknowledgment and References

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□ Related publications

- “Surface-potential Solution for Generic Undoped MOSFETs with Two Gates,” submitted for publication.
- “Explicit Unified Regional Surface Potential for Asymmetric Undoped Double-Gate MOSFETs,” submitted for publication.
- “Compact Modeling of Doped Symmetric DG MOSFETs with Regional Approach,” *Proc. WCM-Nanotech 2006*, Boston, May 2006.
- “Effect of Substrate Doping on the Capacitance–Voltage Characteristics of Strained-silicon pMOSFETs,” *IEEE Electron Device Lett.*, Vol. 27, No. 1, pp. 62–64, Jan. 2006.
- “Extraction of physical parameters of strained-silicon MOSFETs from C–V measurement,” *Proc. ESSDERC 2005*, Grenoble, Sept. 2005, pp. 521–524.
- “Physics-based single-piece charge model for strained-Si MOSFETs,” *IEEE Trans. Electron Devices*, Vol. 52, No. 7, pp. 1555–1562, July 2005.
- “A Compact Model for Future Generation Predictive Technology Modeling and Circuit Simulation,” (*Invited Paper*), *Proc. MIXDES 2005*, Kraków, June 2005, pp. 881–886.
- “Unified Regional Charge-based Versus Surface-potential-based Compact Modeling Approaches,” (*Invited Paper*), *Proc. WCM-Nanotech 2005*, Anaheim, May 2005, pp. 25–30.
- “Single-piece polycrystalline silicon accumulation/depletion/inversion model with implicit/explicit surface-potential solutions,” *Appl. Phys. Lett.*, Vol. 86, No. 20, 202111, May 2005.