Systems & Technology Group,
Technology Collaboration Solutions

BSIM Model for MOSFET Flicker Noise Statistics

Technology Scaling, Area, and Bias Dependence

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Flicker Noise Models

- McWhorter’s number fluctuation (ΔN) theory
  - Carrier release and capture in and out of oxide traps lead to fluctuations in the number of free carriers available for conduction. For uniformly distributed traps (in space and energy), the resulting noise has a 1/f power-spectral density.

$$S_{vg} = \frac{kTq^2}{\gamma f W L C_{ox}^2} N_t(E_F)$$

Cannot explain the increase in Svg with increasing gate bias, typically seen in measured data.

- Hooge’s mobility fluctuation (Δμ) theory
  - All semiconductors exhibit fluctuations in mobility with a 1/f signature. Physical basis can be fluctuations in scattering cross section.
  - Considered to be an empirical, non-physical model.

$$S_{vg} = \frac{q\alpha_H}{C_{ox} W L f}(V_{GS} - V_T)$$

Cannot explain the increase in Svg after the creation of interface traps via hot-carrier stress.

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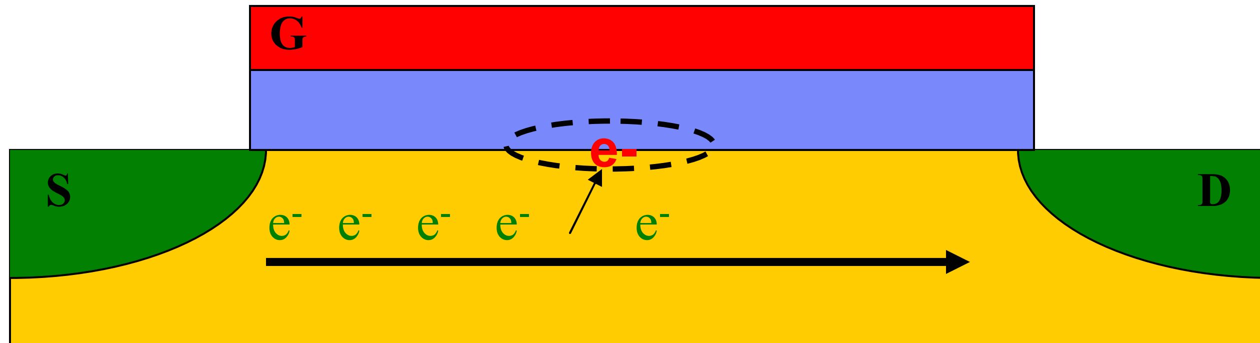
Unified (Correlated) Low-Frequency Noise theory (Nt → ΔN Δμ)



- trapped charge modulates number of carriers (ΔN) and local mobility due to Coulomb scattering (Δμ). Each trapping event leads to a Lorentzian spectrum in drain current.
- for a uniform distribution of trapping time constants, we get an ensemble of Lorentzians that add up to 1/f.

$$S_{vg} = \frac{kTq^2}{\gamma f W L C_{ox}^2}\left(1+\alpha\mu[V_G - V_T]\frac{C_{ox}}{q}\right)^2 N_t(E_F)$$

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Final Formulation in BSIM (since v3.0)

An effective trap density is derived, which produces the observed noise power in the absence of mobility fluctuations.

$$N_t = Noia + Noib \cdot N_{inv} + Noic \cdot N_{inv}^2$$

Noia, Noib, and Noic are extracted from 1/f noise measurements, with the understanding that at high gate bias, Noic and Noib has growing contribution to 1/f noise power.

Noise power calculated in BSIM:

$$Noise\ density = \frac{q^2 kT\mu_{eff} I_{ds}}{C_{ox} L_{eff}^{\ 2} f^{ef} \cdot 10^8}\left(Noia \cdot \log\left(\frac{N_0 + 2\times10^{14}}{N_l + 2\times10^{14}}\right) + Noib \cdot (N_0 - N_l) + \frac{Noic}{2}\left(N_0^{\ 2} - N_l^{\ 2}\right)\right)$$

$$+ \frac{V_{tm} I_{ds} \Delta L_{clm}}{W_{eff} \cdot L_{eff}^{\ 2} f^{ef} \cdot 10^8} \cdot \frac{Noia + Noib \cdot N_l + Noic \cdot N_l^{\ 2}}{\left(N_l + 2\times10^{14}\right)^2}$$

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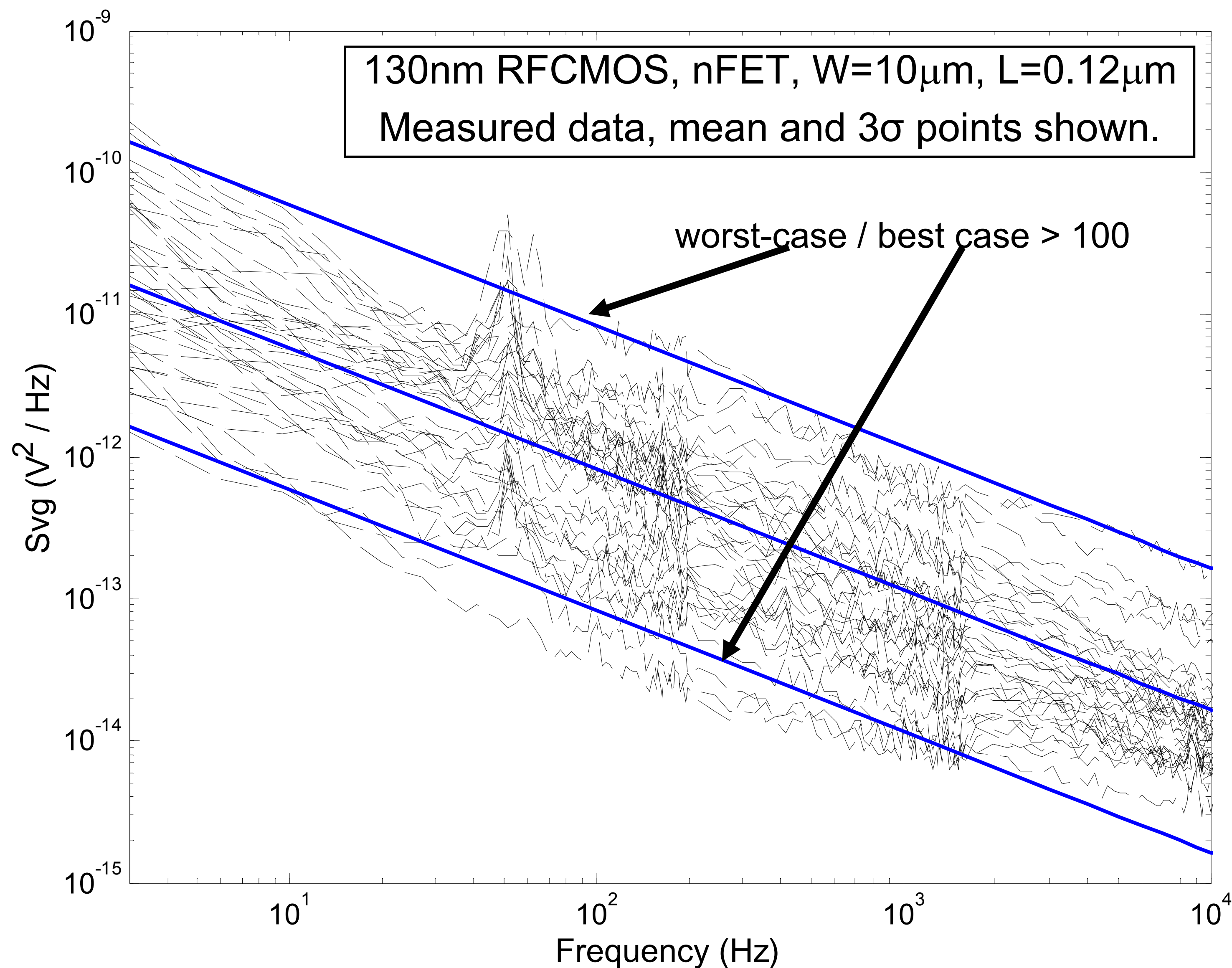
Need for a statistical model (1): Data



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Need for a statistical model (2): Theory & Analysis

- **Most of the variations in S_{vg} come from the variations in N_t (trap density)**
  - N_t is the number of traps per unit area
  - $n_t = N_t * W_i L_i$ is the expected value of the total number of traps in i^{th} device
    - $n_t = \langle n_{t,i} \rangle$
  - $n_{t,i}$ actual number of traps in i^{th} device, will have a Poisson probability distribution

$$P(n_{t,i}) = \frac{{n_t}^{n_{t,i}} \cdot e^{-n_t}}{n_{t,i}!} = \frac{W_i L_i {N_t}^{n_{t,i}} \cdot e^{-W_i L_i N_t}}{n_{t,i}!}$$

  - similarly the effective trap density for the ith device, $N_{t,i} = n_{t,i} / W_i L_i$ will have a Poisson probability distribution.

$$S_{V_G,i} = \frac{kTq^2}{\gamma f W L {C_{ox}}^2} (1 + \alpha\mu [V_G - V_T] \frac{C_{ox}}{q})^2 N_{t,i}(E_F)$$

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Need for a statistical model (2): Theory & Analysis

- **Technology scaling trend: Reducing minimum feature size by 30% cuts the minimum device area in half.**
- **Scaling in analog circuits: Minimum area for a target current level, with noise and mismatch considerations.**

Technology:	Minimum area for Id=1mA @ Vgs=Vds=Vth+0.1V, L=Lmin	approx. # of traps*:
250nm	W=714μm, Area=171 μm^2	8550
180nm	W=141μm, Area=25.4 μm^2	1279
130nm	W=107μm, Area=12.8 μm^2	640
90nm	W=28μm, Area=2.2 μm^2	110

- based on typical trap densities reported in literature, e.g. see Z. Çelik-Butler, "Low-frequency noise in deep submicron metal-oxide-semiconductor field-effect-transistors", IEE Proc. Circuits Devices Syst., Vol. 149, No. 1, Feb 2002

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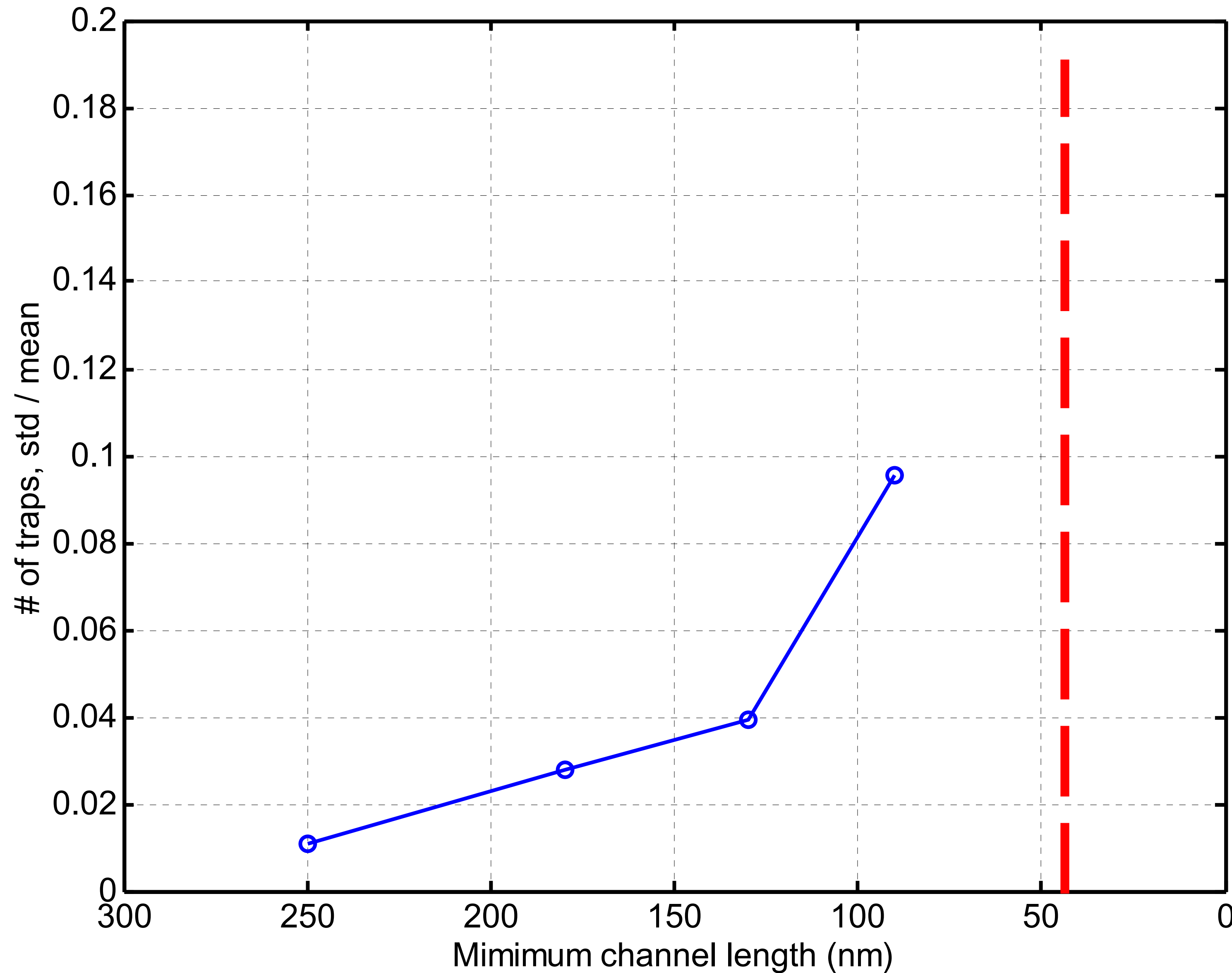
Need for a statistical model (2): Theory & Analysis

The uncertainty in the number of traps and therefore, the uncertainty in 1/f noise power grows with technology scaling.



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180nm and 130nm CMOS Comparison

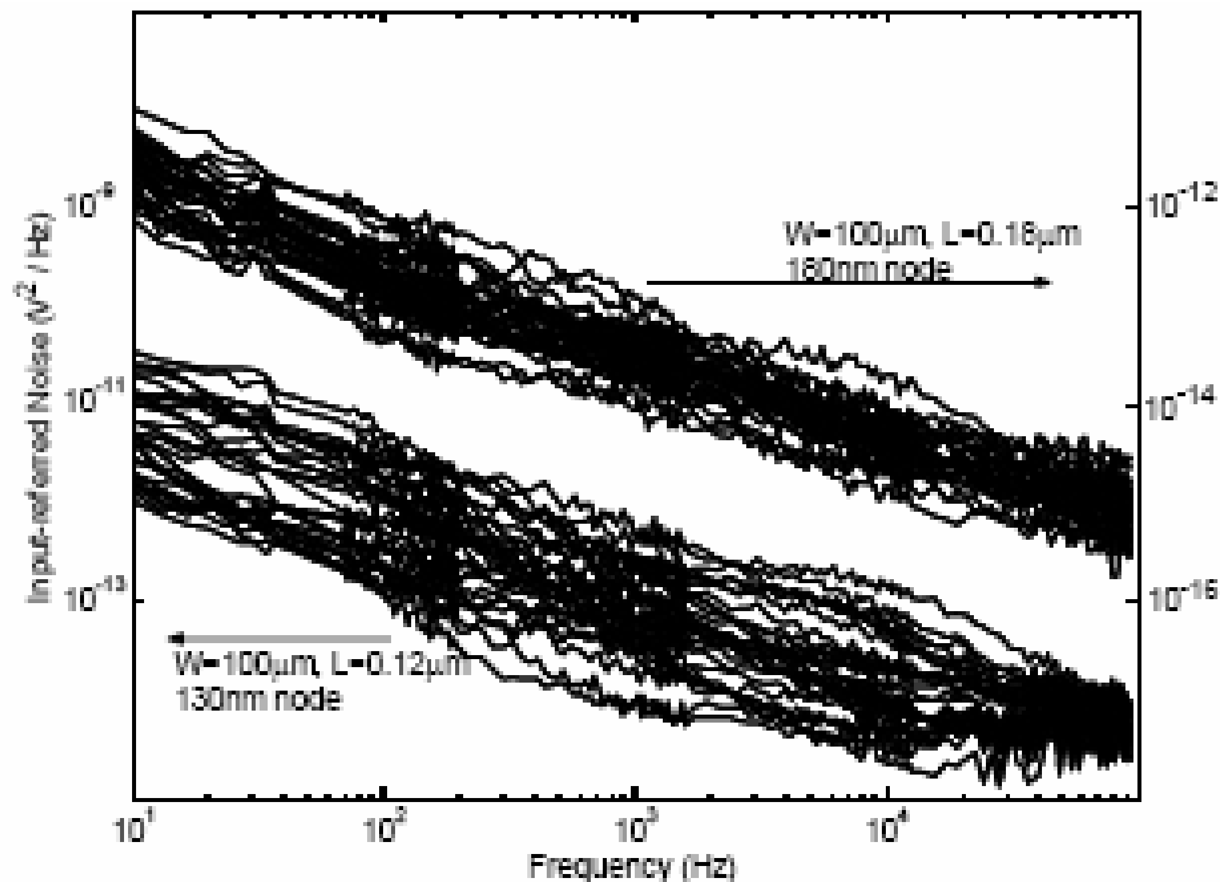

Fig. 1. 130nm and 180nm FETs show similar noise variation. Spread decreases with increased area.

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Statistical Flicker Noise Model Implementation

$$\phi_i = \text{Noise level of i}^{\text{th}} \text{ device}$$

$$k = \frac{\phi_{\text{worst-case}}}{\phi_{\text{nominal}}} = \frac{\phi_{\text{nominal}}}{\phi_{\text{best-case}}}$$

A_0 = area of device k is extracted from (minimum noise variation)

$$M = \ln(k) - \min(\ln\sqrt{\frac{w \cdot l}{A_0}}, 0)$$

D = built in Gaussian variable with mean = 0 and std = 1/3

J = measure of the reduction in noise variation with increasing gate bias.

$$NOIA = A_{\text{nominal}} * e^{D \cdot M}$$

$$NOIB = B_{\text{nominal}} * e^{D \cdot \frac{M}{J}}$$

$$NOIC = C_{\text{nominal}} * e^{D \cdot \frac{M}{J^2}}$$

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Statistical Model to Hardware Correlation

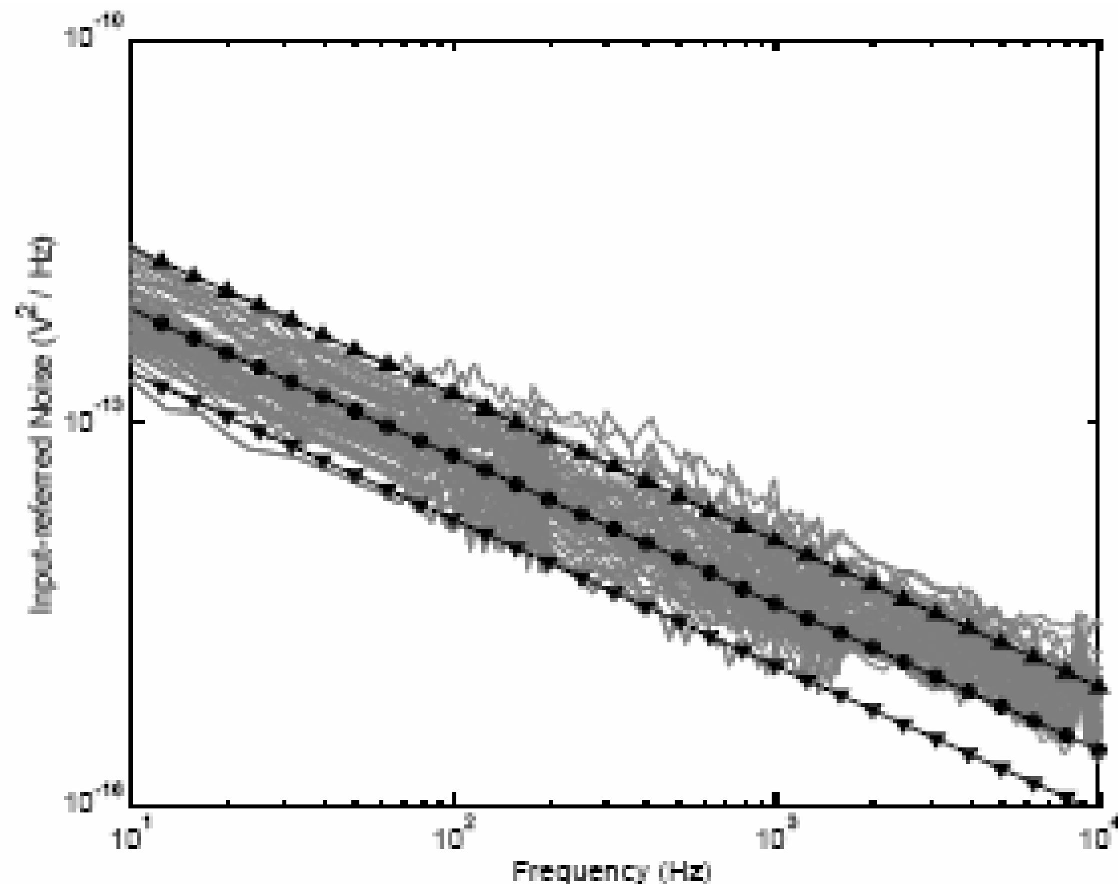

Fig. 2. Nominal, worst-case, and best case; model vs. hardware, pFET W=100μm, L=0.12μm, Vds=1.0V, Vgs=0.41V.

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Statistical Model to Hardware Correlation: Bias Dependence

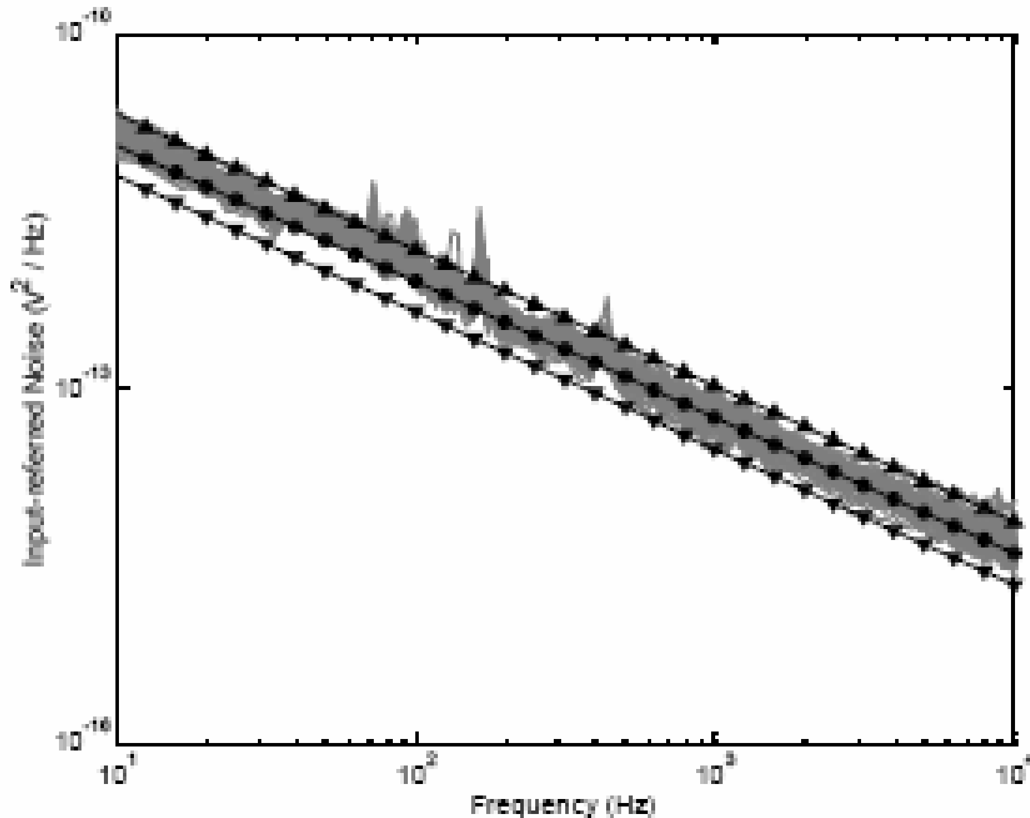

Fig. 3. Nominal, worst-case, and best case; model vs. hardware, pFET W=100μm, L=0.12μm, Vds=1.0V, Vgs=1.17V. Note the reduction in spread at higher gate bias.

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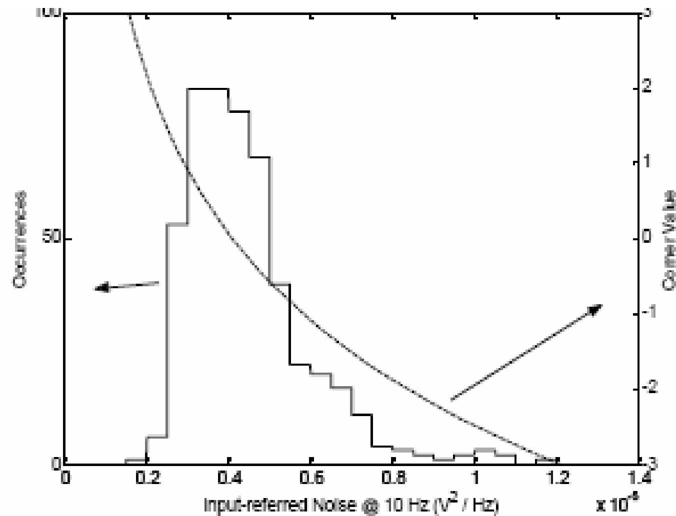

Fig. 4. Monte Carlo and Corner runs, nFET, W=10μm, L=0.12μm, Vds=1.0V, Vgs=0.9V.

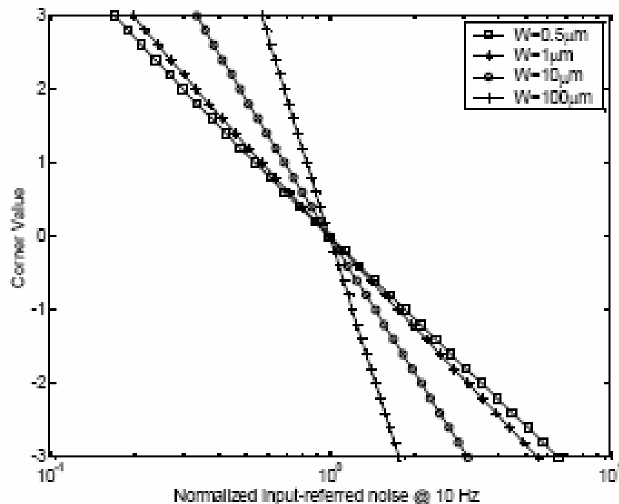

Fig. 5. Corner runs for various gate widths, nFET, L=0.12μm, Vds=1.0V, Vgs=0.7V. Noise is normalized to show relative variation.

- **A statistical enhancement to BSIM noise model**
- **Captures area and bias dependence of noise statistics**
- **Fully integrated into a Process Design Kit**
  - Corner simulations
  - Monte Carlo simulations

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