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SOI CMOS Compact Modeling based on TCAD Device Simulations

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Motivation

- **TCAD simulations have had good success reproducing I-V behavior of SOI devices**
- **Exploit TCAD's predictive capability for early Compact model generation**
- **Potential advantages:**
  - Earlier models for circuit design/evaluation in new technologies
  - More "physical" than compact model fit to old hardware and adjusted to final performance targets

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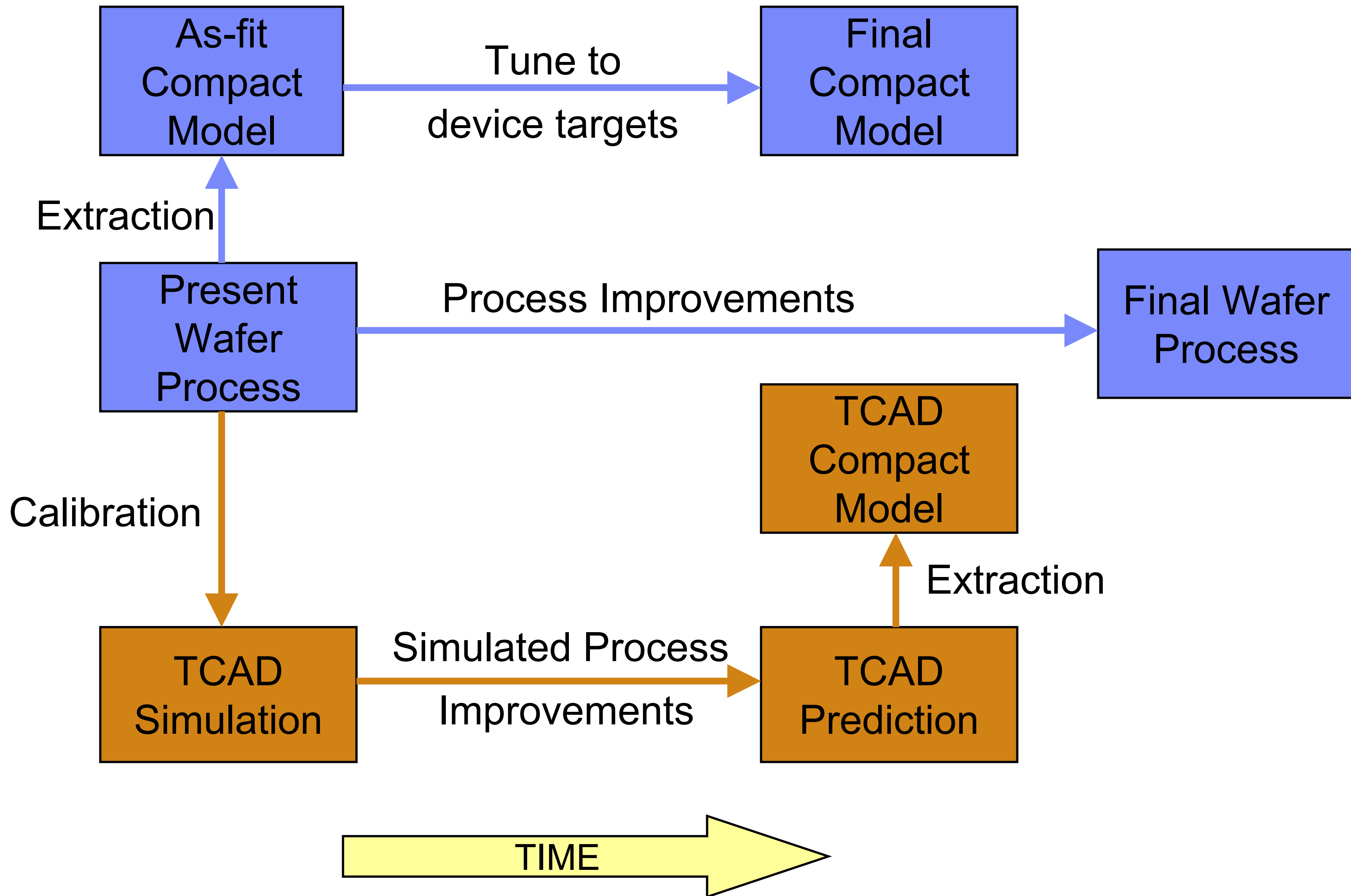
Proposed Role of TCAD



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Model Extraction

Blue = Body-contacted devices

- **65nm node PD-SOI CMOS technology**
- **Compact model: BSIM-PD 2.23**

1) **Junction diode**
2) **Gate current**
3) **Parasitic bipolar**

Low Vds:

4) **Linear VT, Subvt slope**
5) **Low-field mobility (long channel)**
6) **Series resistance (short channel)**

7) **Saturated VT**
8) **Long-channel Idsat**
9) **Short channel Idsat, gds, and Impact ionization**
10) **IDVD (BC and FLT)**
11) **Gate, overlap & junction capacitances**

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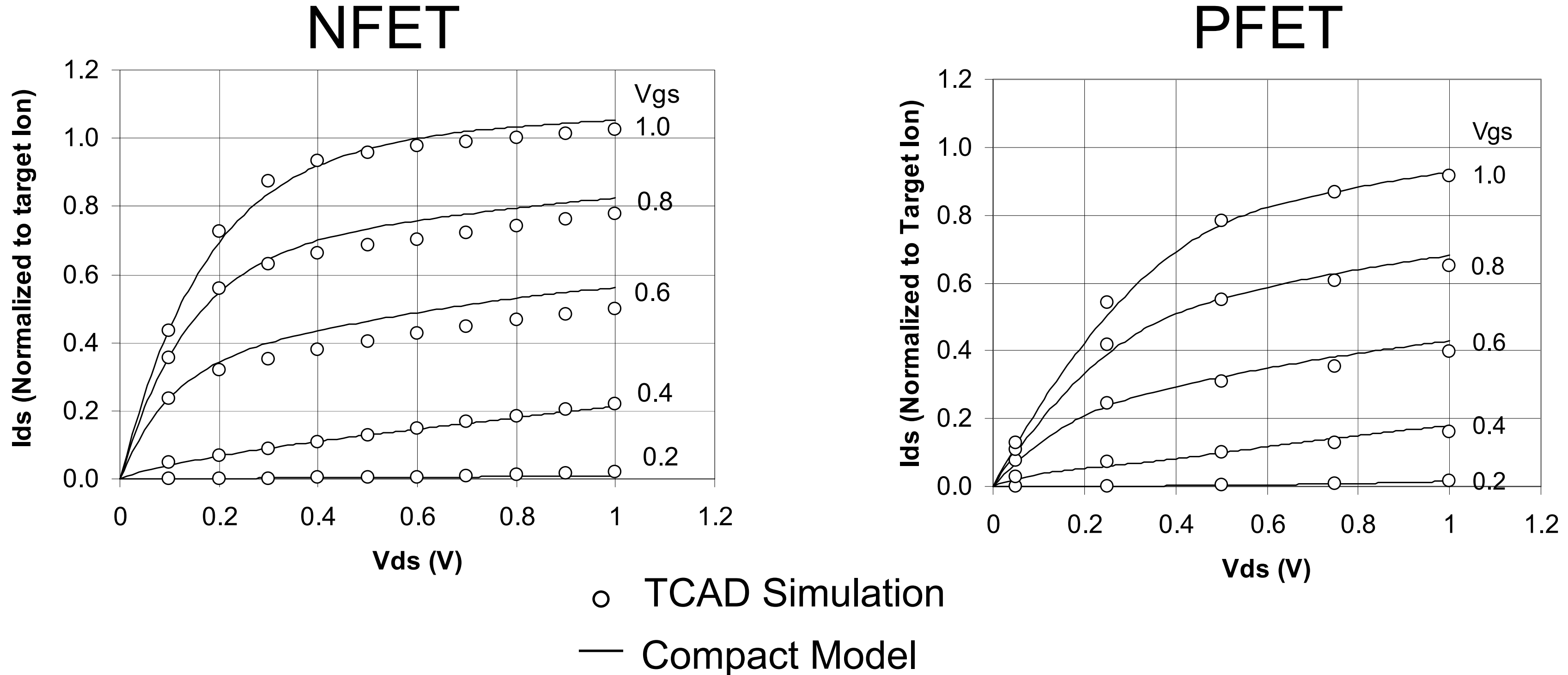
TCAD Simulation vs. TCAD Compact Model



Normalized to technology target Idsat (Vds=Vgs=1.0V)
Floating body

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Conclusions

- **Good fits achieved - promising approach**
- **Imposes stringent TCAD calibration standards**
  - Compact model extraction employs specific bias/geometry conditions to intentionally isolate various physical effects
  - TCAD errors in one region can result in non-physical extracted parameters
  - Interaction of parameters can cause model fitting problems in other regions
- **Suggests improved calibration procedure for TCAD**
  - Bias/geometry conditions as in model extraction

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